Intel Quality System Handbook



August 2006



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1. The Intel Quality Policy

Intel's mission is to "delight our customers, employees, and shareholders by relentlessly delivering the platform and technology advancements that become essential to the way we work and live". Our commitment to quality is an essential ingredient of our corporate culture and values, is a fundamental part of our corporate systems and processes, and is articulated in our Corporate Business Principle:

> **Intent** – Intel's products symbolize world-class leadership in technology and performance, outstanding quality, and lasting reliability. All employees share the responsibility to sustain and improve product quality for our customers.
>
> **Policy Statement** – We strive to maintain the highest standards and ship product that meets our stated goals. If and when a problem arises, we will quickly communicate with our customer on the issue and take action to resolve the problem.

World-class quality leadership is a top priority as semiconductor geometries relentlessly continue to shrink in accordance with Moore's Law. As we design chips with billions of transistors, the real key is world-class manufacturing control and robust design practices working together to produce reliable and technologically superior products. Intel achieves world-class quality through operational excellence, continual improvement, and satisfying customer needs in everything we do. We are committed to delivering the quality and reliability that is worthy of our customers' trust and enables our products to connect people with information and touch lives around the world.



Paul Otellini
President and Chief
Executive Officer

2. Intel's Quality Management System

Nearly 40 years ago, Intel co-founder Gordon Moore forecast the rapid pace of technology innovation. His prediction, popularly known as "Moore's Law," states that transistor density of integrated circuits doubles about every two years. (For more information on Moore's Law, see http://www.intel.com/pressroom/kits/events/moores_law_40th/index.htm.)

The semiconductor industry is a tough proving ground for a company's commitment to quality. Intel's status as a global leader in semiconductor manufacturing relies upon a relentless pursuit of defect reduction, and a tremendous investment in innovation to deliver ever-increasing value to our customers.

Intel's brand name stands for technology and safety worldwide. Intel pursues innovation and improvement in all of our business processes, systems, and methods. Rather than simply detect and correct defects in the later stages of production, Intel strives to build quality and reliability into every step of our design, development, and manufacturing processes. The Intel Quality Management System provides the framework to meet the challenges of this competitive and innovative environment.

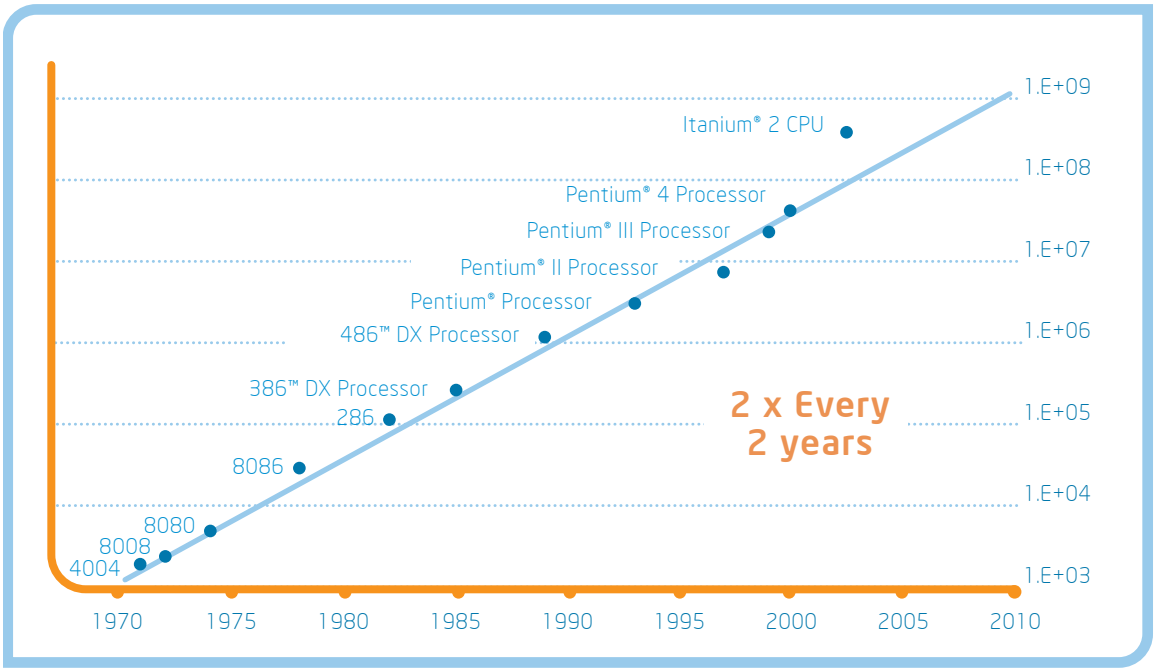


Figure 2-1: Microprocessor Transistor Count

2.1 Quality Management System (QMS) Framework

Intel established the Quality Management System (QMS) as the foundation for customer satisfaction and continuous improvements in all aspects of our business. The quality management system is based on the customer-supplier relationship and provides a framework for managing the activities used to develop and deliver quality products that consistently satisfy customer and other external requirements. QMS is deeply rooted in Intel's culture, our corporate mission and values, business principles, actions, and results. Improving QMS is an ongoing process throughout Intel organizations.

2.2.1 Intel's Mission and Values

Intel's QMS begins with the responsibility of management to define how the organization will conduct business. Intel's corporate mission and values statements guide these business plans.

Intel's Mission — Delight our customers, employees, and shareholders by relentlessly delivering the platform and technology advancements that become essential to the way we work and live.

Intel's Corporate Values — Intel's corporate values and supporting behaviors provide employees with effective ways to create a work culture that strongly supports Operational Excellence. Our values of Customer Orientation, Discipline, Quality, Risk Taking, Great Place to Work, and Results Orientation define Intel's commitment to excellence in both the marketplace and the work place (Figure 2-2).

VALUE	SUPPORTING BEHAVIOR
Customer Orientation	Listen and respond to our customers, suppliers and stakeholders Clearly communicate mutual intentions and expectations Deliver innovative and competitive products and services Make it easy to work with us Be vendor of choice
Discipline	Conduct business with uncompromising integrity and professionalism Ensure a safe, clean and injury-free work place Make and meet commitments Properly plan, fund and staff people Pay attention to detail
Quality	Achieve the highest standards of excellence Do the right things right Continuously learn, develop and improve Take pride in our work
Risk Taking	Foster innovation and creative thinking Embrace change and challenge the status quo Listen to all ideas and viewpoints Learn from our successes and mistakes Encourage and reward informed risk-taking
Great Place to Work	Be open and direct Promote a challenging work environment that develops our workforce Work as a team with respect and trust for each other Win and have fun Recognize and reward accomplishments Manage performance fairly and firmly Be an asset to our communities worldwide
Results Orientation	Set challenge and competitive goals Focus on output Assume responsibility Constructively confront and solve problems Execute flawlessly

Figure 2-2: Intel's Values and Supporting Behaviors

Through these values and the behaviors, Intel seeks to:

- Continuously improve the customer-perceived value of our products, processes and people
- Continuously improve our efficiency in performance of all activities
- Continuously reduce our total cost of doing business

2.1.2 Intel's Quality Policy

Intel's management is committed to the integration of quality principles into our management systems. They have established a clear quality policy and embedded it in our corporate business principles. Refer to Intel's Quality Policy in Section 1.0 for details.

2.1.3 Elements of Intel's QMS

Intel's Quality Management System consists of four key elements: 1) Plan, 2) Organize, 3) Execute, and 4) Monitor (Figure 2-3). Intel uses these elements to achieve customer satisfaction by driving our management processes and providing a framework for ensuring predictable and consistent planning, development, quality, and service support. Intel's QMS promotes customer focus, clear management responsibility, a process approach to doing work, and continuous improvement of the system.

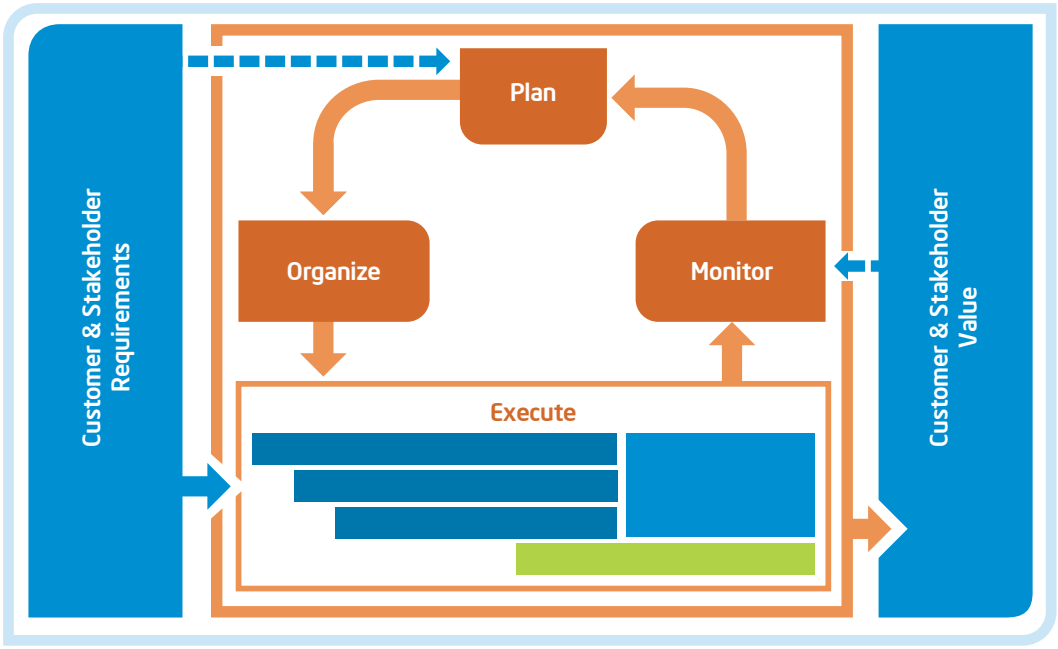


Figure 2-3: Intel's Quality Management System Elements

Plan — Quality is the result of proper planning and regularly reviewing and adjusting plans. Intel management uses the Corporate Planning Process (Figure 2-4) to review organizational performance for customer and market needs, and to direct changes in the way we perform work. The Corporate Planning Process begins with a current situation analysis that identifies areas needing strategic focus. This involves a variety of tools and activities, such as customer satisfaction surveys and competitive benchmarks. The Corporate Planning Process also uses assessments of our future direction, our industry, the economy, environmental trends, and other factors. With this information, Intel prepares to develop or revise our strategic long-range plan. Typically encompassing a three- to five-year outlook, the strategic long-range plan serves as the basis for Intel's annual plan.

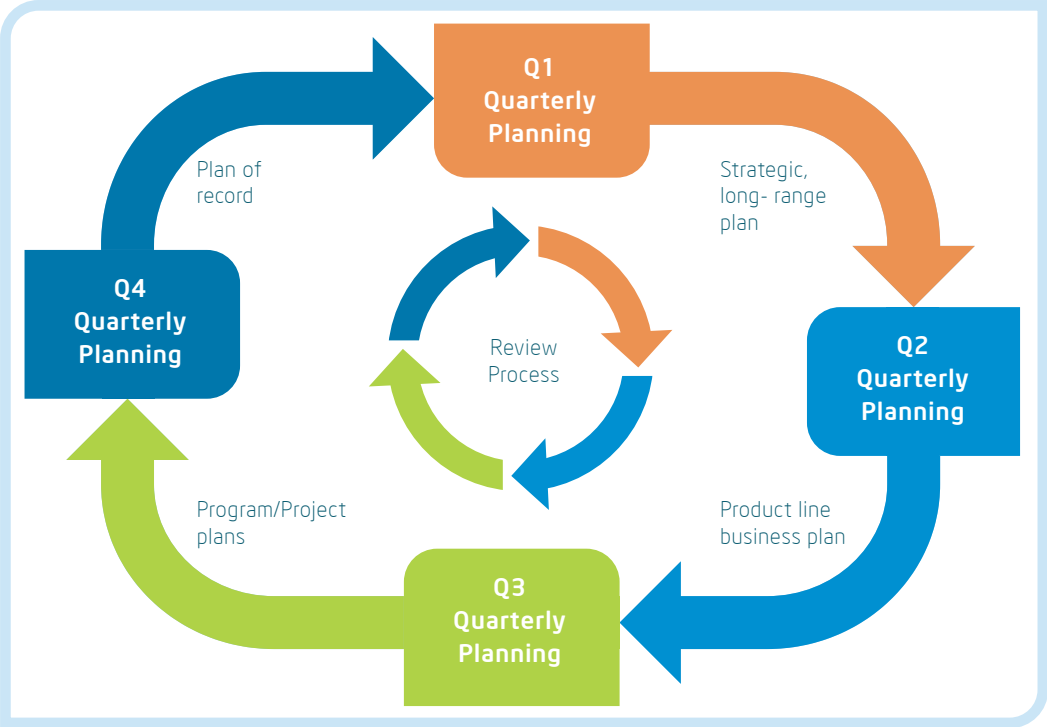


Figure 2-4: Corporate Planning Process–Strategic Planning Cycle

The annual product-line business plan identifies corporate objectives for each business group. Business groups then define strategies and tactics to meet corporate objectives. The approved tactics evolve into projects and programs that form the plan of record. Intel evaluates these plans on a quarterly basis to track progress.

This planning sequence—situation analysis, strategic long-range planning, annual planning and quarterly reviews—ensures that individual employee, department and group plans positively affect our corporate business objectives. Plans nest vertically in the organization and resources align cross-functionally to optimize the interfaces between organizations.

Organize — Resource management is required to carry out the organization's work for satisfying customer quality needs and maintaining the system. The scope of resource management includes chartering of groups to do work, and providing funding, people, training, tools, and methods.

Intel sets the project priorities and allocates resources (money and people) based on business priorities. This funding method, combined with specific planning processes, aligns the quality resources necessary to achieve business objectives down to the project level.

Intel University develops and delivers training, utilizing both internal and external resources, to upgrade the skills and knowledge of all employees. Employee training courses include quality and reliability concepts, methods, and tools. The Corporate Quality Network's (CQN) College of Quality (COQ) provides these training courses through the Intel University systems to employees worldwide.

Execute — This QMS element encompassed the activity needed to create Intel's products and services and deliver them to its customers. Structured business processes define how to execute work across all major operations in the company. Intel's five major operations are (Figure 2-5):

- **Technology Development** — Enables Intel's products to provide better value through improved performance, increased functionality, or smaller size
- **Product Development** — Processes used to take a product from market research through production and eventually to product discontinuance
- **Materials Management** — Provides materials and services for production to meet agreed upon requirements, lead times and pricing
- **Manufacturing** — Enables quality production by understanding customer quality requirements and implementing processes that help ensure operations meet these requirements
- **Customer Support** — Provides customer assistance by understanding, documenting, analyzing, and resolving customer issues



Figure 2-5: A Functional View of Intel's Major Operations

These five major operations integrate to form the "Execute" element of Intel's QMS. Each operation has a quality management system that performs the quality related functions as shown in Figure 2-6.

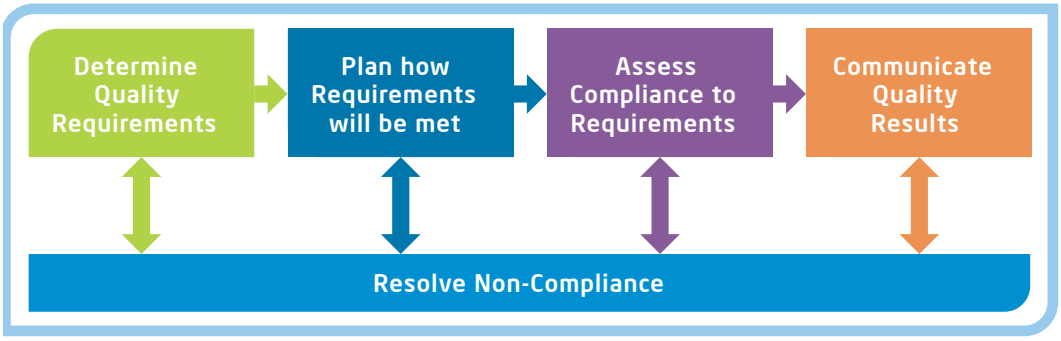


Figure 2-6: Quality Related Functions

Monitor — Intel's Quality System provides the framework for ensuring predictable, consistent product planning, product development, product quality, and quality service support. Intel regularly reviews how well we deliver value to our customers and we believe that strong business results are our ultimate measure of success.

We regularly monitor and evaluate results from all of our key operations, processes, products, services, customers and suppliers. Based on these evaluations, quality management teams understand opportunities for improvement, prioritize actions, and provide resources. Execution teams may address one or more specific issues as part of their charter.

Figure 2-7 shows the overall relationships between Intel QMS elements, and the operations and functions they support. Chapters 3 through 7 provide further details on the quality systems supporting each operation.

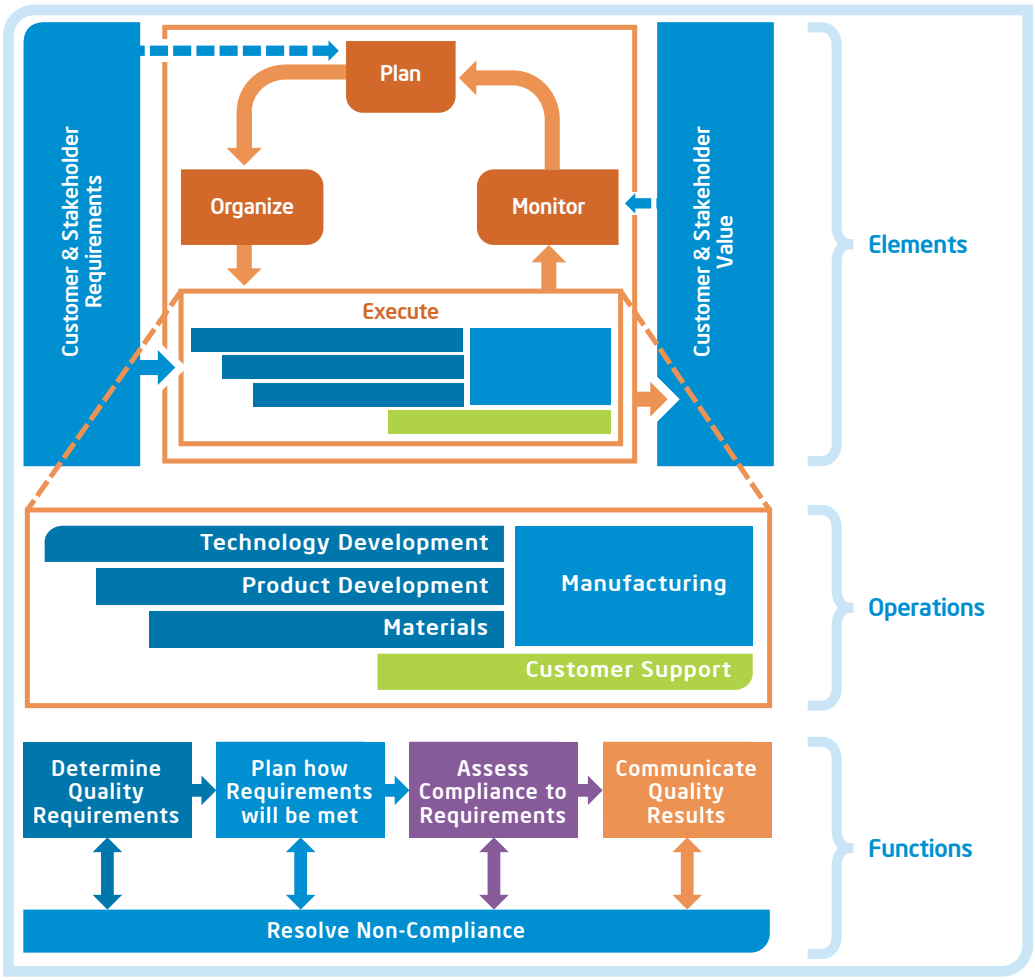


Figure 2-7: QMS Elements, Operations, and Functions

2.2 Quality Documentation System

Intel's quality documentation system is comprised of a document structure hierarchy and a network of document control centers.

2.2.1 Document Structure

Figure 2-8 shows Intel's document structure. Moving from the top of this structure downward, documents become more specific in their purpose and scope, and document content becomes increasingly detailed.



Figure 2-8: Quality Document Hierarchy

Corporate Business Principles represent Intel's leadership principle and occupy the peak of Intel's document structure. They are guidance for making key decisions and apply to all Intel employees through group guidelines.

Group Guidelines are high-level requirements for achieving synergy across operations, and consist of major policies/guidelines, high level requirements and organizational roles and responsibilities.

Governing Specifications are requirements to achieve synergy across operations and groups, and include detailed methodologies, best-known methods, specific criteria, requirements, and roles and responsibilities. These roles and responsibilities govern operational policies and procedures and apply to several operations in a business group or across business groups.

Operational Policy/Guidelines are requirements to define roles and responsibilities, and requirements for a specific operation or function within a business group.

Operational Procedures are systematic instructions, details of execution and supporting information for a specific operation or function within a business group.

2.2.2 Document Control

Intel has an extensive system for ensuring quality documentation using document control and engineering change control. The Document Control Management System incorporates requirements for quality assurance, assessment, and improvement. It encompasses specifications that represent the cumulative technical expertise of design, development, and manufacturing activities.

Corporate Document Control acts as a centralized focal point for developing, implementing, standardizing, and controlling Intel specifications worldwide. It also provides guidelines to over 50 satellite Document Control Centers (DCCs). DCCs are located at Intel facilities to support geographically dispersed organizations, and DCC guidelines indicate minimum requirements for controlling and handling Intel documents. Each DCC supplements the guidelines with requirements specific to local organizational and customer needs.

Control of Quality Records — Intel maintains quality records that demonstrate the effectiveness of our quality system and achievement of required quality system standards. Quality records are critical tools for analyzing results and trends. They not only enable us to determine the need for corrective action, but also help us track ongoing improvements.

Intel has established procedures for identifying, collecting, indexing, filing, storing, maintaining, and disposing of quality records. Quality records for a given product—whether centrally located or retained by individual organizations—are identifiable, retrievable, and legible. Intel's Corporate Records Management has procedures for submitting records to off-site storage and for retrieving them. These procedures also state minimum record retention periods. Quality records in electronic format are available on-line and are subject to regular backup according to documented procedures.

3. Technology Development

Technology Development produces a set of core technologies shared by many Intel products. Intel utilizes combinations of silicon technologies, package technologies, test technologies, and board technologies to bring products to market.

- **Silicon Technology** — The fabrication process used to create integrated circuits (IC) on silicon wafers by adding and patterning the layers that form transistors and interconnects.
- **Package Technology** — The assembly process used to enclose silicon ICs in an electronic package with connections accessible to the user.
- **Test Technology** — The test process, from wafer sort through package-level test and burn-in, designed to ensure that shipped devices meet quality and data sheet requirements.
- **Board Technology** — The design and fabrication of printed circuit boards using multiple components.

3.1 Moore's Law and the Impact of Scaling

Nearly 40 years ago, Intel co-founder Gordon Moore forecasted the rapid pace of technology innovation. His prediction, popularly known as "Moore's Law," states that transistor density on integrated circuits doubles about every two years. Today, Intel continues to lead the industry, driving Moore's Law to increase functionality and performance and decrease costs, bringing growth to industries worldwide. For additional information on Moore's Law, refer to http://www.intel.com/pressroom/kits/events/moores_law_40th/index.htm.

In addition to the progress made in silicon technologies, generational advancement has occurred in package, test, and board technologies. For example, as processor performance increases with improvements in process technologies, the demand on packaging solutions also increases. Device input/output (I/O) requirements increase the number of connections of chip-to-package or within a package (Figure 3-1), and also increase demand on package interconnects to deliver more complex thermal, power delivery, and signal integrity solutions.

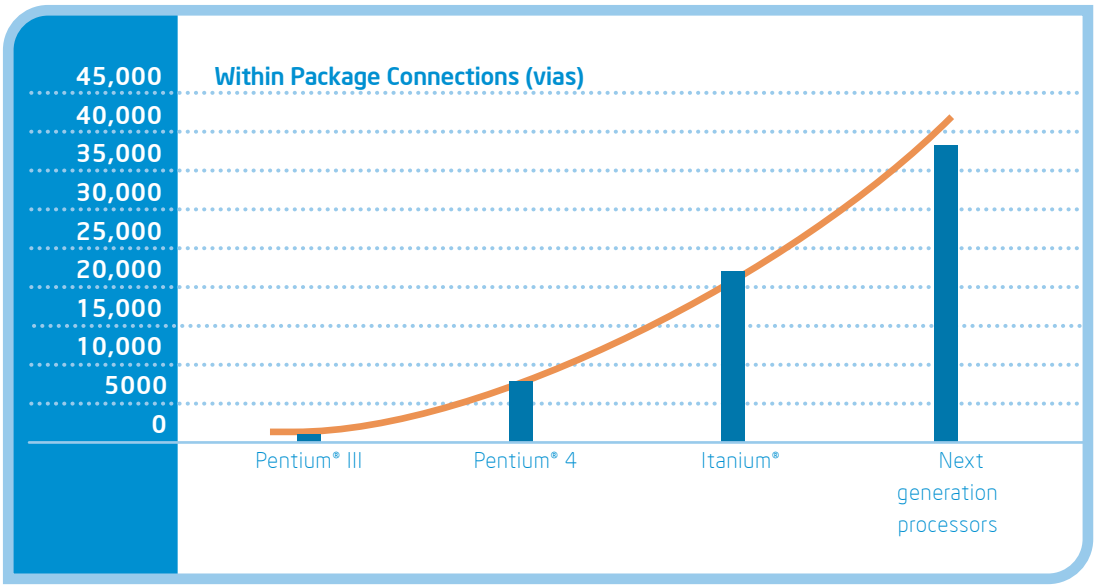


Figure 3-1: Increasing Chip to Package Connections

Smaller transistors consume less power, but as transistor density and speed rise, the chip consumes more overall power and generates more heat. In addition, leakage — the continued flow of current even when the transistor is "off" — becomes more problematic, wasting a higher portion of total device power. Power densities are increasing exponentially and the thermal impact to quality and reliability is growing in complexity. To meet this challenge, Intel has developed a variety of novel power-saving techniques, such as new transistor structures and materials, innovative approaches to circuit and micro-architecture design, and advanced packaging materials and system components.

3.2 Technology Development to Production

Developing and certifying new processes for wafer fabrication, package, test, and board manufacturing is the responsibility of Intel's Technology Development organization. Technology certification ensures the quality and reliability of the technology and that interactions between technologies (for example, between a silicon technology and a packaging technology) are understood.

Technology development occurs in four distinct phases: Pathfinding, Definition, Development, and Deployment.

The **Pathfinding** phase involves exploration of product needs and understanding the options for design, material, process, and equipment.

During the **Definition** phase, the Technology Development organization selects options and develops technology and business plans to satisfy Technology Target Specifications. In parallel, the quality and reliability organization develops certification plans to achieve the reliability requirements. Technology Development determines if the needed materials and infrastructures exist or can be developed in time to support the targeted product.

In the **Development** phase, the development site establishes an initial process or test flow. The flow is characterized and the findings are used to refine and optimize the process. Reliability characterization is an integral part of this iterative process; key learnings are fed back to the Technology Development team for process optimization. When a technology meets the yield, manufacturability, reliability, and performance goals on a test vehicle and lead product the technology is certified and moves into Deployment.

In the **Deployment** phase, the certified technology is transferred to manufacturing sites and ramped into production. Intel's Copy Exactly! methodology (Section 6.3) ensures that a technology is transferred identically to all Intel manufacturing sites. Matching includes process parameters, yields, and reliability results. This approach allows Intel to ramp new technologies quickly across multiple locations, enables each site to share what they learn for continuous improvement, decreases production ramp time, and improves product availability.

Figure 3-2 illustrates the phases of Technology Development.



Figure 3-2: Phases of Technology Development

3.2.1 Stress-Based and Knowledge-Based Testing

Reliability certification and product qualification utilize combinations of stress-based testing and failure-mechanism based testing. Stress-based testing refers to the use of standardized stress conditions, durations, and success criteria (e.g., JEDEC Standard JESD47). Failure-mechanism testing (also known as knowledge-based testing) refers to the use of customized stresses that accelerate known failure mechanisms, such that the qualification or certification emulates a product usage at some specific conditions of product usage. JEDEC Standard JESD94 describes this approach. This approach requires knowledge of the failure mechanism and its acceleration model and knowledge of how to detect the failure mechanism.

Although stress-based testing has strong historical precedence, its one-size-fits-all approach may fail to detect some mechanisms and over-accelerate others. For example, a standard 1000-hour, 125°C life-test will fail to detect mechanisms with no temperature acceleration (such as flash memory SILC-related charge loss) and yet emulate thousands of years of usage (at 55°C) for a mechanism that has high temperature dependence. Standards based approaches may inadequately comprehend the difference between the usage conditions across various types of products.

Data on failures or parametric shift behaviors is used to derive reliability models during initial characterization of the new technology. Failure analysis, along with other materials analysis tools, is used to assess the physics of failure. The acceleration factor relationship between the accelerating variables is established by applying the mathematics that describes the physics of failure. For example, Intel may describe materials degradation in various bake temperatures and, by regression, fit them to an Arrhenius relation. The residuals analysis indicates how well the regression model matches the data. When the correct form and parameters for the reliability model are established, product use conditions are substituted into the model to make reliability estimates.

Figure 3-3 describes the sequence of actions and evaluations that lead to the final reliability stress conditions and durations.

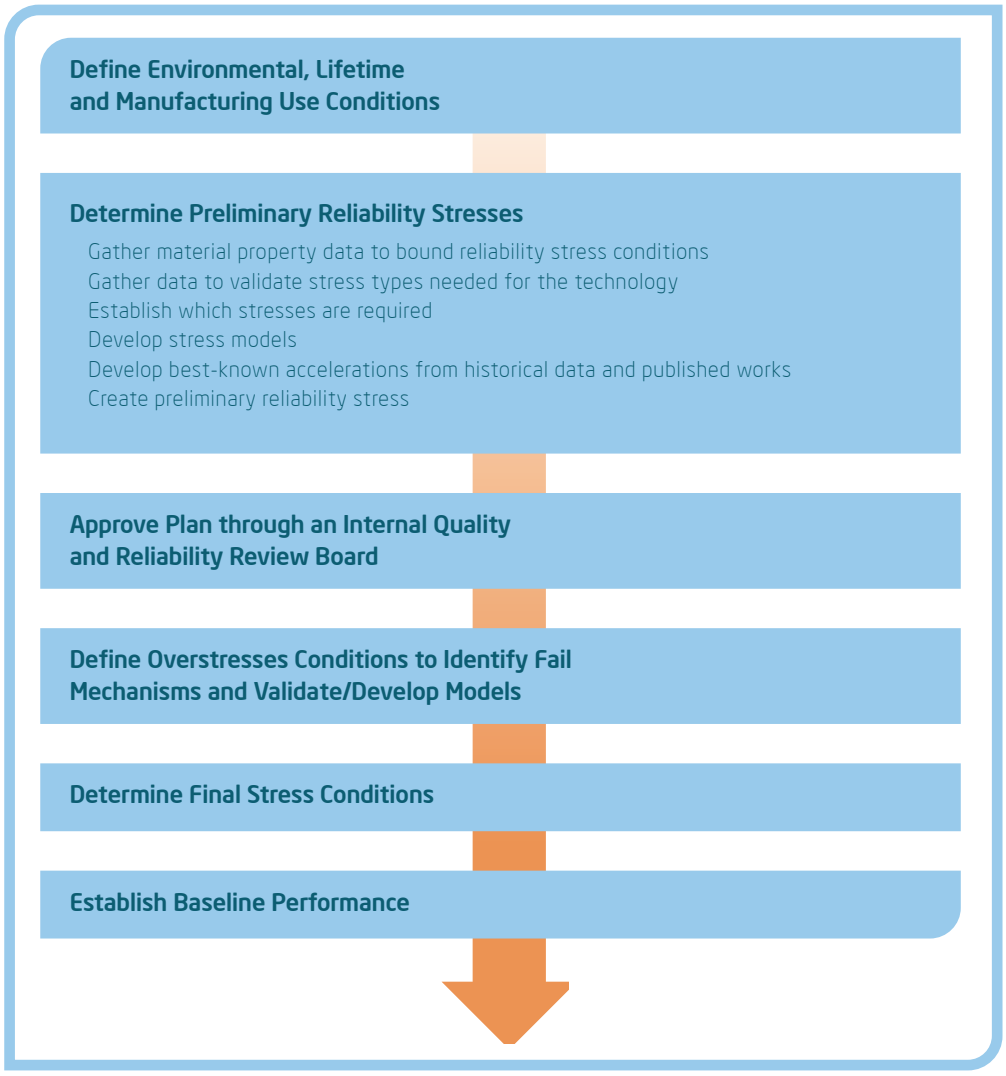


Figure 3-3: Reliability Stress Conditions and Durations

Historically, semiconductor device physics used a knowledge-based approach in such areas as electromigration, hot carrier degradation, and gate oxide integrity, where specialized test structures are used to detect a particular failure mechanism. A mix of standards-based and knowledge-based approaches has been used for many years in product qualifications. For example, qualification life-tests often use a standard requirement of 1000 hours at 125°C, but results have been extrapolated to 55°C operation based on knowledge of the activation energies for the failure mechanisms. Intel certifications include reliability evaluations that use stress conditions based on targeted product use conditions and failure mechanisms, rather than obtaining them from following a prescribed table of stress conditions in a specification. For more information, see http://www.intel.com/design/packtech/245162.htm.

3.3 Silicon, Package, and Test Technology Certification

Intel certifies a process technology when it meets quality and reliability goals, and the lead product has been manufactured on the technology and shown to meet requirements.

3.3.1 The Silicon, Package, and Test Technology Development Flow

During the **Pathfinding** phase, Intel compiles quality and reliability requirements for silicon and package technologies. These are based on customer expectations, product use conditions, technology features and risks. Test technology pathfinding starts with test equipment capability studies to ensure test issues are identified.

In the **Definition** phase, methods and tools are selected. Critical parameters for design, test and manufacturing are defined and key specifications are developed. Reliability target specifications for process modules (short sequences of process steps) are defined based on the quality and reliability goals and the technology characteristics. For test technology, target specifications and critical success indicators are defined. Quality and reliability test vehicles for silicon and package technologies are selected and developed. These include test devices and structures for silicon technology and test vehicles for package technology. Selections for test equipment, tooling and material are finalized.

In the **Development** phase, processes are established and refined to meet the technology target specifications. Characterizations are conducted for silicon and package technologies including detailed analyses of failure mechanisms and failure rates. Quantitative failure models are developed (Section 3.2.1) and overall process reliability is verified by characterizing failure populations and kinetic behaviors on representative devices. As the development moves forward, characterization results are fed back into the development cycle to refine the reliability target specifications, stress methods, metrologies, sampling and test plans. Interactions between technologies (such as silicon-to-package interactions) are also characterized. When yield, reliability, module and test vehicle metrics demonstrate process stability and process control, a pre-certification baseline is achieved. As additional material is processed, a growing base of process performance data is gathered and compared to the pre-certification baseline. When adequate baseline performance is demonstrated, the test vehicle is certified. At this point samples for customer design evaluations and customer manufacturing line qualifications become available.

In the final phases of development, critical process steps are evaluated by additional process window characterizations. Typically, these characterizations utilize test vehicles to measure the effects of process and design rule variations on reliability performance. Lead product tests are concluded, and process control parameters and systems are finalized. The Development phase concludes when a silicon, package or test technology achieves certification based on substantial manufacturing, yield, quality, and reliability data.

In the **Deployment** phase, the certified technology is ramped into high volume manufacturing. Silicon, package, and test processes are transferred from development to manufacturing sites using the Copy Exactly! method. With Copy Exactly! the receiving manufacturing site fully integrates the new technology into volume production while matching the critical attributes of the certified process. Process matching includes critical-step process control capability and stability, yield, in-line monitor data, quality and reliability performance. In a typical silicon process matching, over 20,000 control parameters are considered. (See Section 6.3 for more about Copy Exactly!) Transfer certification is achieved when parameters are matched on a large sample of processed material.

Technology certification reports and enabling component (e.g., socket) validation reports are completed after certification. The reports document the certification, validation sample size, and estimates of reliability based on stated market use conditions and other information. Intel performs enabling validation on most reference designs and publishes results in the form of thermal and mechanical design guidelines. Contact Intel Customer Support for more information.

3.3.2 Key Challenges to Certification of Logic Technology Processes

Bringing advanced silicon technology processes to market is subject to a variety of electrical, thermo-mechanical and environmental reliability considerations and risks. For example, electrical effects leading to contact degradation, electromigration, gate oxide leakage and changes in transistor circuit characteristics must be considered. Thermo-mechanical mechanisms caused by temperature cycling or moisture changes are also important. Environmental risks such as electrostatic discharge events or the effects of ionizing radiation are also key considerations. Understanding these types of reliability risks and developing the tools and techniques to assess them define the key challenges for silicon technology certification.

3.3.3 Technology Development Tests and Mechanisms

Intel's technology certifications consist of a combination of standards-based testing and failure mechanism-based testing (Section 3.2.1). Failure mechanism-based testing requires understanding the specific failure mechanisms, including derivation of acceleration factors or activation energies. The following are examples of stress tests and failure mechanisms:

High temperature and voltage operating electrical life tests measure the impact of latent defects on early-life and late-life reliability and the onset of intrinsic failures in late-life. These tests functionally exercise the device at elevated junction temperatures and multiple voltages to accelerate failure mechanisms. The data is used to derive acceleration factors and construct proprietary quantitative technology models for the early-life and late-life portions of the product life curve. Then statistical comparisons of products to the model are made to validate if the product behaves according to the model.

High temperature bake with no applied voltage tests evaluate the early-life and late-life reliability impact of high temperature storage without electrical bias, in conformance with the procedures defined in JEDEC Standard JESD22-A103-B. This stress accelerates failure mechanisms such as C4 joint degradation, ionic contamination, contact integrity, and metal void propagation.

Highly accelerated stress tests (HAST) uses high temperature and high humidity stress to evaluate early-life and late-life moisture reliability of non-hermetic devices, according to procedures defined in JEDEC Standards JESD22-A110-B and JESD22-A-118. This stress accelerates moisture-related failure mechanisms such as metal corrosion and contamination-induced threshold shifts. These tests complement highly accelerated stress tests on test chips biased at multiple voltages. Based on the resulting data, Intel develops proprietary quantitative failure models and compares them to product data.

Temperature cycling evaluates the early-life and late-life mechanical integrity of the device when exposed to temperature extremes, in conformance with procedures defined in JEDEC Standard JESD22-A104-B or JESD22-106-A. This stress accelerates mechanical failure mechanisms such as solder joint fatigue, package cracking, and interlayer dielectric cracking in the die and package.

Soft error testing is performed on test vehicles at specialized facilities. Soft errors are caused by ionizing radiation passing through the circuit. The resultant charge upsets the balance of logic nodes. This radiation originates from two sources: alpha particles from the radioactive decay of materials employed in component fabrication and high-energy neutrons from intergalactic sources.

Latch-up testing determines product sensitivity to parasitic bipolar action in CMOS technologies. Intel tests parts functionally and parametrically after stress using an automated tester. Tests include voltage latch-up to determine the product sensitivity to V_{CC} over-voltage and input/output (I/O) latch-up to determine product sensitivity to pin overshoot and undershoot.

Electrostatic Discharge (ESD) tests measure a product's sensitivity to electrostatic damage. The human body model (HBM) test simulates human handling. This type of event occurs when a person transfers a charge from their body into a device. Intel uses the ANSI/ESDA Standard Test Method 5.1 Specification to determine the HBM test conditions. The charged device model (CDM) simulates mechanical handling. This type of event occurs when a device accumulates charge during automated handling and is discharged to a low resistance, low inductance ground plane. Intel uses the ESDA Draft Standard Practice to determine the CDM test conditions.

Electromigration causes the interconnect resistance to increase during use and can result in circuit failure. Current in metal lines and vias causes motion of metal ions in the direction of electron flow. This motion can result in void formation at points of flux divergence and can cause resistance increases. If the forces produced by the ion motion exceeds the limits of the surrounding dielectric, extrusion formation may result leading to shorts to adjacent structures. Intel evaluates electromigration mechanisms using specialized test structures that represent the physical structures allowed by design rules. Failure population statistics and kinetics are characterized using elevated temperatures and current densities.

Time dependent dielectric breakdown is a gate dielectric failure resulting from gate leakage current. Failure kinetics depends on applied voltage bias and temperature. Intel develops proprietary quantitative failure models based on data from accelerated stress testing.

Hot carrier injection occurs when hot carriers, produced by impact ionization, are accelerated toward the gate by the applied electric fields. This causes CMOS transistors to suffer an increase in trapped oxide charge and interface state density at the drain end of the channel. The resulting changes can cause circuit failures such as timing faults or latch stability faults. Intel performs stresses on simple circuits in AC and DC, various transistor dimensions in DC, and integrated circuits (e.g. SRAM and microprocessors) in AC. Failures are defined as a change in transistor or test circuit characteristics or a failure to meet data sheet specifications. Proprietary quantitative models are developed based on test data collected before and after each accelerated stress.

Bias temperature instability is an important reliability issue for PMOS transistors in the negative bias condition. These transistors suffer an increase in interface trap density and positive fixed oxide charge. The resulting changes can cause circuit failures such as timing faults or latch stability faults. Intel defines a failure as a change in transistor or test circuit characteristics consistent with design rules, or a failure to meet data sheet specifications.

3.3.4 Key Challenges to Certification of Flash Memory

Technology certification methods for flash memory technologies are similar to those used for other silicon technologies. The main differences are in reliability stresses related to flash endurance and retention. Endurance is the ability of a flash memory to survive repeated program/erase cycles. Retention is the ability of a flash memory to retain data over time, with or without power.

Intel bases endurance and retention certification requirements on use conditions for the product. Use conditions include considerations for the physical environment (e.g., temperature) and the software environment (e.g., number and frequency of block erasures, number of read/write cycles, etc). Use condition models are derived from actual and hypothetical studies and include guard banding. Intel's certification requirement is for failure rates to be low for the targeted use conditions and with no wearout.

Table 3-1 summarizes key endurance and retention reliability stresses. Intel characterizes flash memory endurance up to the maximum cycle count (typically 100K cycles) and across the full minimum/maximum operating-temperature range (typically -40°C to +85°C). Retention is characterized before and after endurance cycling using unbiased retention stresses ("bakes") as well as biased stresses ("disturbs"). Retention stress temperatures typically range from room temperature to 140°C with data typically collected for 1000's of hours, in some cases collected for years.

Stress	Description	Detected Failure Mechanisms
Early cycling endurance	Very large sample size cycling to 10 cycles	Defects responsible for endurance infant-mortality failures
Extended cycling endurance	Large sample size cycling up to maximum datasheet specification	Defects responsible for random-life failures Intrinsic dielectric trapping leading to program/erase slowdown
High-temperature retention, uncycled	High-temperature bake and high-voltage life test	Temperature-accelerated defects
Room-temperature retention, uncycled	25 degrees Celsius unbiased retention test using margin-voltage acceleration	Non-temperature-accelerated defects
High-temperature retention, cycled	High-temperature bake on cycled units	Dielectric charge detrapping
Room -temperature retention, cycled	25 degrees Celsius unbiased retention test using margin-voltage acceleration, on cycled units	SILC-related dielectric leakage leading to charge loss or charge gain
Read disturb	25 degrees Celsius retention test with positive gate bias, on uncycled units	SILC-related dielectric leakage leading to charge gain

Table 3-1: Flash Failure Mechanism

Endurance Testing — Endurance issues for infant mortality, random life, and wear-out often follow a bathtub curve. Table 3-1 includes two endurance stresses used by Intel.

Early cycling endurance testing cycles every cell in a very large number of devices to ten cycles. This test is used to detect low defect levels of infant morality related mechanisms.

Extended cycling endurance testing cycles blocks to various fractions (up to 100%) of the maximum cycles allowed by the data sheet. This test is used to resolve random-life and wear-out issues.

In actual use, only a fraction of the blocks in any device will cycle to 100,000 cycles, and cycling every block is impractical for a certification. Intel develops use conditions models by measuring cycling in actual usage. For example, studies of cell phones, PDA's, and data cards reveal that most blocks cycle to only a fraction of the maximum specification. All blocks generally experience some cycling, and many experience moderate amounts of cycling, but only a fraction experience the maximum number of cycles per the data sheet. The information from these real scenarios and from hypothetical usage scenarios are used to derive use models and subsequently the endurance test conditions.

Retention Testing — Retention failure mechanisms for flash memories have a wide variation in properties, especially their temperature and voltage accelerations. Multiple types of retention tests are used to ensure all mechanisms are detected.

Traditionally, tests are based on EPROM retention mechanisms discovered in the 1970's and 1980's, that have activation energies of about 0.6eV. These mechanisms can be detected by life tests at 125°C and bakes at 140°C to 150°C. Intel performs these traditional bakes on uncycled devices to detect these mechanisms.

Today's flash memories operate in the Fowler-Nordheim tunneling regime, and are susceptible to tunneling-related retention mechanisms that have little temperature acceleration. High-temperature bakes can actually heal some defects rather than accelerate them, as is the case of the Stress-Induced Leakage Current (SILC) mechanism. Room temperature retention testing is used to detect tunneling-related mechanisms such as SILC (on cycled devices) and process related defects (on uncycled devices).

Margin-trend extrapolations are used to estimate lifetime. (Margin refers to the difference between a cell's threshold voltage at a particular measurement time and the threshold voltage at which the sense amplifier would detect a failing cell.) Margin data is taken over time and extrapolated to the full retention requirement using physical models for this behavior.

Detrapping mechanisms have a very high activation energy of about 1.1eV. This is the dominant mechanism found by using an unbiased, high-temperature retention test on cycled devices. Bake temperatures and times are chosen to represent the required field retention requirement.

Charge gain, caused by bias to the top gate of the flash cell during the read operation, is a mechanism that can occur during extended operation under bias. Charge gain is usually a result of tunneling and therefore has little temperature acceleration. Two retention tests target charge-gain effects:

- *For uncycled devices* in high-voltage life-test, the read gate voltage is elevated compared to actual use.
- *For cycled devices*, gate-bias stresses use special test modes that bias the gates of all cells to high simultaneously (as compared to the real-usage case in which only one row out of many thousand would be biased at any one time). This provides acceleration without relying on temperature. In this case, the dominant mechanism is SILC-related leakage.

For retention, flash memories should endure years of use without failures caused by data loss. For example, a block written with code should hold that code for the full product lifetime without losing a single bit of data. For this reason, use condition models comprehend multi-year retention for blocks written at the beginning of the product's life.

There are also retention failure mechanisms that originate only through defects generated by program/erase cycling. For such blocks, the relevant use-condition models comprehend how many cycles a block receives, how long it takes to acquire that many cycles, and how much retention time will lapse after the cycling completes. Hypothetically, if the cycling stops altogether, flash memory should retain data for the lifetime of the product. Use conditions for these types of use scenarios comprehend retention times in actual usage plus guard bands based on hypothetical usage scenarios.

3.3.5 Key Challenges to Package Certification

Increasing product and market performance needs drive process and design development for package, assembly, and enabling processes. New products typically require feature size reduction and added design complexity to accommodate improved functionality and increased electrical requirements. Physical design complexity translates into mechanical and thermo-mechanical effects. Stringent electrical requirements result in higher current and power density and higher electrical fields. The development and validation of reference designs for the heat sink, socket, and board also have increasing design complexity and performance-driven requirements.

Package, assembly, and enabling processes must be synchronized with silicon process and product development, as well as board and system development. New product requirements drive additional complexity into all aspects of technologies used in finished products. Intel uses a combined technology risk assessment approach during development—where all technologies are simultaneously exercised—to identify and test interactions and enable a successful integrated product qualification.

To allow product design flexibility, packages and assembly processes are characterized using design and process window characterizations to establish the technology envelope, form factor ranges, and design rule envelopes.

Enabling validation is performed on mechanical reference designs, sockets, and heat sinks to provide the customer with proof of concept. Accelerated environmental reliability stresses such as bake, temperature cycle, and moisture test are used for enabling characterization and validation. The output of the enabling validation is contained in validated thermal-mechanical design guides available at http://developer.intel.com. Validated socket reports are available from the respective Intel-qualified socket suppliers.

3.3.6 Key Challenges to Test Certification

Electrical testing ensures product functionality at the required speed and that the product meets Intel's quality goals. Test processes also provide valuable feedback to the upstream silicon and assembly processes, often detecting subtle variations in product performance parameters, such as defect density, frequency, power, etc. Test feedback is used to reduce variations and improve upstream processes.

Each generation of process technology and product design can double or triple the number of transistors in a product. This growing complexity demands constant improvement in test capability and capacity and efficient use of test resources is such ways as:

- utilizing design for test features, e.g., enabling very high speed array tests
- designing in redundancy to increase fault tolerance
- improving tester hardware architecture, e.g., optimizing design and hardware to enable parallel device testing
- safely reducing test content, e.g., eliminating redundant or ineffective content and replacing with quality monitors.

In addition, extensive optimization of product test flows, equipment layout, and software automation are used to minimize the complexity of manufacturing while ensuring high quality products.

Market needs for increased product performance, higher functionality, environmental compliance, and lower cost are significant factors in developing new silicon, package, and board technologies. Anticipating and planning for the impact of these factors on testing requires creative solutions and improvements for issues related to:

- increased product power densities, particularly at burn-in
- increased mechanical fragility due to low-k dielectrics, lead free metallurgy, and thin packages
- increased ESD sensitivity (reduced capacitance for higher performance)
- increased off current (i-off) of new technologies impact on burn-in power

3.4 Board Technology Certification

Ever increasing demands for higher product performance drive board technology development and certification. Certification activities include the validation of new enabling components and thermal solutions, as well as board reference designs. Advancements in silicon technology act as the primary driver of board technology developments. For example, an increase in the power consumption of silicon devices necessitates the need for more efficient thermal dissipation solutions. Additionally, increases in the number of inputs and output for the packaged component drives needs for pitch reduction.

Many options are available to achieve increased board performance. These include feature size reduction (both at the component and board level) and increased complexity in board design. Generally, the changes that produce increased functionality and overall system performance also affect the requirements for thermal and mechanical performance. During board technology development and certification, Intel focuses primarily on ensuring that the stringent requirements for board level interconnect are met.

To minimize the occurrence of potential manufacturing issues during launch of new board products or technologies, a Customer Manufacturing Enabling (CME) team engages directly with board manufacturers and system integrators. This engagement may involve the direct transfer of process technology information, working with the manufacturer to set-up and characterize their assembly line, or troubleshooting fabrication problems. Industry readiness assessment is a required element for technology certification. Overall, board certification and product qualification must demonstrate that:

- All quality and reliability requirements are met
- Technology stability and capability targets are met
- Product performance meets all requirements
- Industry capability assessment completed for product ramp

Intel places emphasis on continuous improvement of the methodology via post-launch data collection, customer feedback, and internal development activities. Capability development and enhancements, such as refining reliability models, creating new predictive simulators, and improving knowledge of product use conditions, also contribute to the Board Technology Development Flow from a quality and reliability perspective.

3.4.1 Board Technology Development Flow

The board technology development quality and reliability efforts involve close collaboration with internal development groups in other functional areas (e.g., package technology, enabling components, test technology) to deliver a robust integrated solution that meets the market needs.

Pathfinding — During Pathfinding, Intel identifies many technology options and evaluates them from manufacturing, quality, and reliability perspectives. In the next phase, Intel performs additional development on those technologies that represent the best candidates for meeting performance, manufacturing, quality, and reliability requirements.

Discovery — During the Discovery phase, selected technology options are narrowed based on modeling and empirical data collection. Critical inputs and options affecting materials, process, and design selection are evaluated. Failure Mode and Effects Analysis (FMEA) is used to document anticipated failure mechanisms that require special attention during reliability testing. In general, only technologies representing high confidence solution paths are carried into Development. The Discovery phase ends with which technologies will be developed and their associated certification strategies.

Development — Intel refines and documents critical attributes on materials, assembly processes, and design as requirements to meet technology certification targets. A detailed reliability certification plan is defined based on known or anticipated failure mechanisms. Execution of this plan involves completion of all required data collection by the use of test vehicles or reference design boards. Intel optimizes process materials specifications, board assembly processes, and design rules through this testing. A risk assessment methodology monitors progress against the certification requirements and goals. Finally, Intel completes verification of failure mechanism assumptions and validates reliability models before certification is achieved.

Deployment — Certification of the individual manufacturing sites is a major milestone during Deployment. Sites must meet all defined requirements as a requisite to site certification. Intel expects each factory to demonstrate performance that is equal to or better than the baseline established during Development.

3.4.2 Certification Reports

Upon completion of technology certification, sites generate a report summarizing the methodology used to validate the quality and reliability requirements for the board platform. The report explicitly defines the technology envelope covered by the certification testing. This testing is accomplished using test vehicles designed at Intel. Included in the certification report are reliability test requirements and goals, sample sizes, and test results. This report also describes the actual reliability test details and the stress conditions to exercise specific quality and reliability attributes. This report is available to Intel customers through their Customer Quality Engineer (CQE) representatives.

3.4.3 Key Challenges to Board Certification

The requirements of new products for an ever-increasing level of performance and capability drive an associated higher level of complexity in all technologies for that product. For board level technologies the key challenges for reliability include thermal and mechanical performance. For example, scaling reduction in package pitch will generally lead to a decrease in margin for solder joint reliability. Decreased solder fatigue resistance and greater susceptibility to mechanical shock or vibration damage may manifest this during shipping or end use. Similarly, the increasing power consumption of silicon components requires more efficient thermal solutions for heat dissipation. Mounting of these thermal solutions onto the circuit board becomes more difficult and overall mechanical reliability is more problematic since the trend is to increase the mass of the heatsinks. Additionally, the introduction of new board and chassis form factors are major modulators of mechanical robustness. Generally, Intel identifies these types of issues early in the Discovery phase of the technology lifecycle through the FMEA process. Capturing of these technology issues is important to allow sufficient time for understanding root cause, inherent risk, risk mitigation or corrective actions).

Another key challenge involves obtaining a thorough understanding of the product usage. The usage models and associated use conditions are important in defining the types of stress testing necessary to demonstrate achievement of reliability requirements. Moreover, setting appropriate product goals links directly to the product use conditions. Development of predictive reliability models also relies on an understanding of use conditions. As new applications are developed for Intel's technologies (i.e., new usage models), it becomes necessary to understand and develop use condition models. This task is not trivial and requires a high level of technical expertise and data collection capability. Compared to standards-based testing, performing evaluations based on a use condition methodology provides a superior assessment of the reliability attributes of the technology.

4. Product Development

Intel delivers on the Intel brand promise in the markets we serve through a commitment to achieving undeniable quality and reliability leadership. The Product Development organization responds to this commitment through the Product Qualification System and the Validation Process. The results are qualified products that achieve the stated quality goals prior to revenue shipment.

4.1 Product Qualification System

Intel meets a wide range of new challenges to maintain world-class product quality and reliability even as product complexity and performance steadily increase. Intel anticipates and addresses these challenges using the Product Qualification System (PQS) to deliver products that consistently meet the quality and reliability goals across different usage segments.

The PQS system provides the framework to:

- Apply the product quality and reliability requirements
- Develop and apply engineering solutions through the Design In Quality and Reliability (DIQR) process
- Validate product performance through reliability stress testing, quality testing, and safety and regulation checks for the finished product
- Deliver meaningful collaterals to our customers
- Release healthy products into Intel's world-class manufacturing system

Figure 4-1 illustrates the Qualification System Architecture, its closed loop nature, and the relationships between elements.

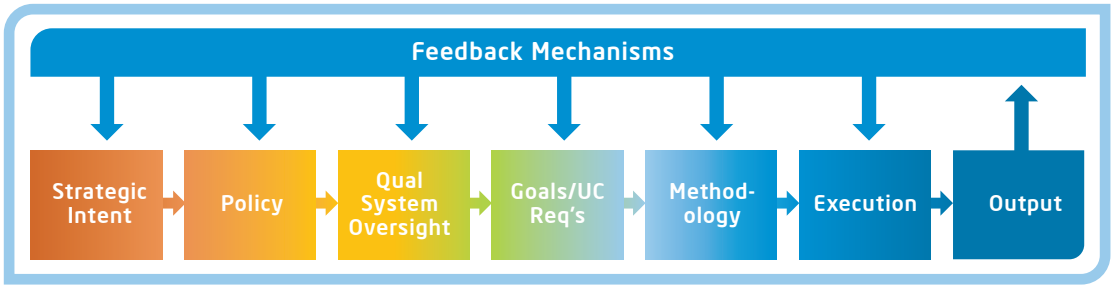


Figure 4-1: Product Qualification System Architecture Elements

The elements of the Product Qualification System Architecture are:

- **Strategic Intent** — the Corporate Quality Business Principle documents the objective for quality and reliability leadership
- **Policy** — high-level requirements to achieve qualification synergy across organizations in response to the Strategic Intent
- **Qualification System Oversight** — how the Qualification System is managed
- **Goals/Use Condition Requirements** — establishes and maintains product quality and reliability requirements
- **Methodology** — high-level process to manage product quality and reliability risk from inception to end-of-life
- **Execution** — the identification, development, and performance of the evaluations required for product health
- **Output** — qualified products, their associated qualification results, and the mechanisms for sharing this information with our customers
- **Feedback Mechanisms** — processes for input from product quality and reliability evaluations, internal stakeholders, and external customers in order to drive continual improvement

4.2 Intel Product Life Cycle

The Intel Product Life Cycle (PLC) is an integrated approach to the major phases of a product's life including exploration, planning, development, production, and eventual discontinuance (Figure 4-2). It involves all operations and levels of the organization. Management approvals are required to move from one phase to the next.

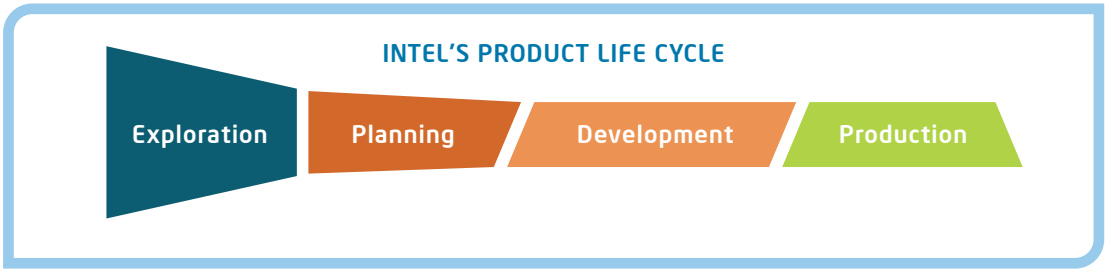


Figure 4-2: Intel's Product Life Cycle

- **Exploration** — a product or product family opportunity is evaluated
- **Planning** — a program Plan of Record (POR) is established to enable the organization to commit funding and resources to the project
- **Development** — a Product Development Team develops the product to meet its requirements and validates product quality
- **Production** — Manufacturing, Sales, Customer Support, and Service Support production availability, the program is evaluated for key learnings, and eventual product discontinuance

4.3 Product Qualification and the Intel Product Life Cycle

Successful product qualification relies on a series of evaluations designed to validate performance to the quality and reliability goals. Intel tracks the advancement of qualification activities and milestones through the PLC phases (Figure 4-3). These milestones shape and drive the requirements, establish the development expectations, and result in qualified products. Validation, the process of proving product and platform designs, is performed in parallel with the product qualification process.

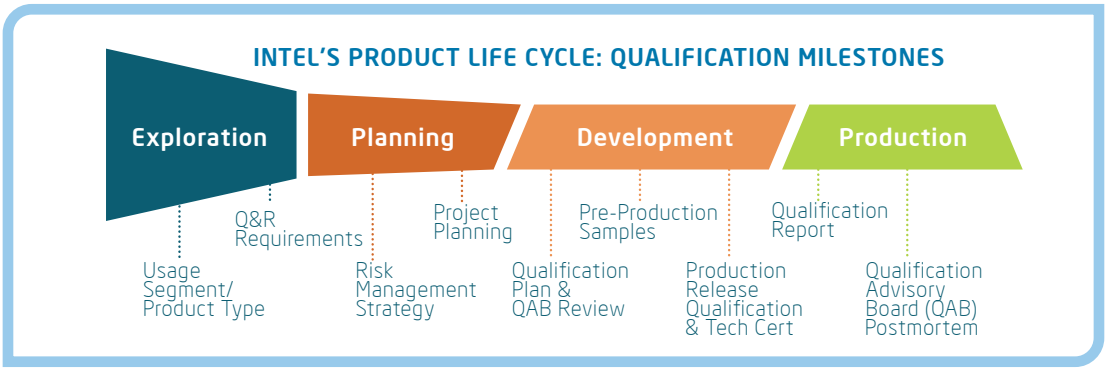


Figure 4-3: Product Qualification PLC Milestones

4.3.1 Exploration Phase

Usage Segment Milestone — Intel classifies product applications into usage segments. Groups of products that have similar usage conditions and characteristics such as product lifetime, ambient temperature, thermal cycling, soft error resilience or shock and vibration exposure define usage segments. Determining the usage segment early in the product lifecycle helps frame the overall product quality and reliability expectations. Examples of usage segments are:

- Mobile Personal Computer
- Wireless Handheld Devices
- Desktop Client Personal Computer

- Workstation Personal Computer
- Consumer Personal Computer
- Enterprise and Carrier Grade Server
- Telecom Controlled Environment
- Telecom Uncontrolled Environment
- Industrial
- Embedded Products

Q&R Requirements Milestone — In the Exploration phase, a product is designated for use in one or more of the segments. As the Exploration phase continues, a comprehensive set of quality and reliability goals and use conditions are developed. Information from customer surveys, third parties, usage measurement studies, and hypothetical usage scenarios are considered. National and international regulatory compliance is also taken into account. The result is a quality and reliability qualification plan and risk assessment strategy that is integrated into the product requirements document.

4.3.2 Planning Phase

Risk Management Strategy Milestone — In the Planning phase of the Product Life Cycle, technical challenges (risks) are identified and evaluated. Therefore, product qualification can be viewed as a risk management and risk mitigation or reduction process. For example, a reliability stress such as temperature cycling evaluates the risk of thermal cycling triggering a failure mechanism. If the mechanism occurs, the risk during normal operating conditions needs to be quantified. An initial strategy would be based on factors including information from similar qualified products and from the silicon and package technology certifications. The strategy would include identifying possible failure mechanisms, developing failure acceleration methods, and ensuring the needed test and analytical tools are available. During the Development phase, data would be collected to quantify the risk, and measure the effects of mitigation and corrective actions. The risk level must be reduced to a low level of risk to achieve qualification of the product.

Project Planning Milestone — The key output from the planning phase is a product implementation plan that includes all the elements for successful qualification:

- Critical product success indicators
- Required resources including headcount, expenses, capital costs
- Tasks and tools needed, such as reliability calculators, Computer Aided Design (CAD) tools and flows, and reliability stress equipment

4.3.3 Development Phase

Qualification Plan and QAB Review Milestone — Early in the Development phase, the Qualification Approval Board (QAB) reviews the qualification plan to ensure it is complete and accurate. The plan includes the quality and reliability requirements, the risk management strategy, and qualification execution details. It documents how the product will be evaluated to meet the product data sheet characteristics, usage segment goals, customer needs, and industry standards. Key plan elements include the pre-silicon qualification plan and the quality and reliability validation plan.

Pre-Silicon Qualification Plan — The Pre-Silicon Qualification Plan (PSQP) defines how Design for Quality and Reliability methods is applied to the product development process. Key methods include Correct-by-Construction, Design for Reliability, Reliability Verification, Design for Test and Design for Manufacturing. These methods employ a CAD tool or a best known method (BKM) or both. (A BKM is a process of making and checking designs using a proven workflow and checklist.) CAD tools - including DIQR tools - go through a certification process to ensure they are effective, accurate, and have adequate coverage and performance.

Correct-by-Construction — In order to ensure that reliability design rules and goals are met during design, Correct-By-Construction tasks such as power-grid planning for electro-migration, signal routing for joule heating, and verification of cell libraries are performed.

Design For Reliability — BKMs are applied to assure the product design has robust reliability performance for ESD protection, latch-up performance, gate dielectric reliability, hot carrier reliability, and threshold voltage stability.

Reliability Verification — Design databases are verified for compliance to the reliability design rules through automated reliability verification checks. Regardless of styles of designs (custom design, analog, ASIC or SOC), each undergoes verification steps at multiple hierarchy-levels (block and full chip). For example, design rules are developed and checked for electromigration/joule heating, ESD, Latch-up, IR drop and signal integrity, hot carrier effects, negative bias temperature instability, antenna charging, and thin film cracking.

Design for Test — BKMs ensure the product is testable to Intel's test coverage standards and incorporate features to accelerate the qualification process. These methods include structural testing of memory and logic, quiescent current measurements, and guard banding rules and techniques. DFT also incorporates features into the silicon design to accelerate product development such as silicon debug, fault isolation, and fault tolerance schemes.

Design for Manufacturing — BKMs ensure the product is manufactureable through waver fabrication and assembly processes, whether in house or outsourced. These methods comprehend Fab, Design for Burn-in, Design for Assembly, Design for Packaging, and Design for Debug.

Quality and Reliability Validation Plan — The QRV contains the details of how the quality and reliability will be validated. It includes the list of stress assessments, sampling plans and success criteria. The assessment strategy is to compare the reliability behavior of the product to the expected baseline behavior. The assessment plan also includes how other available, relevant data may be applied. Other data may come from relevant product qualifications or technology certifications.

Pre-Production Samples (PPS) Milestone — Pre-Production Samples become available when the product has completed a substantial portion of the qualification plan activities. This milestone allows our customers to obtain representative samples of production material to enable their application and manufacturing qualification processes. Pre-production samples have very limited availability, carry a special mark and are not covered by Intel's product warranty.

Production Release Qualification (PRQ) Milestone — At Production Release Qualification, the qualification plan is complete, the supporting technologies have been successfully transferred to manufacturing, and factory control systems are in place. At PRQ, Intel ships commercial products that meet Intel's quality and reliability requirements and are supported by Intel's product warranty.

4.3.4 Production Phase

Product Release Qualification Report Milestone — Product Release Qualification reports formally document a product's performance as prescribed in the Qualification Plan, including meeting the data sheet characteristics, applicable usage segment goals, customer needs, and industry standards. Additionally, the applicable process certification reports are referenced, and all reports are retained to meet customer documentation requirements and for internal continuous improvement.

Qualification Approval Board (QAB) Postmortem Milestone — All Product Development Teams conduct a formal qualification postmortem. The Qualification Approval Board, or equivalent body, collects and consolidates product qualification postmortem results. This final milestone completes a feedback loop that provides two important benefits. First, it captures learning from product generation to generation, which can be applied to future product qualifications. Second, it provides feedback about the qualification system to drive system improvements.

4.4 Validation

Validation, the process of proving product and platform designs, is performed in parallel with the product qualification process. We believe we maintain the industry's most advanced and comprehensive testing environment. Thousands of employees in more than 20 facilities around the world are dedicated to validation testing, and to delivering the world's most reliable and compatible computing and communication platforms. Refer to the Intel Platform Validation Lab Tour at http://www.intel.com/design/chipsets/labtour.htm for more information about validation.

Validation teams focus on both pre-silicon and post-silicon methods. Pre-silicon validation aligns with the Planning and early Development phases of the product life cycle while post-silicon validation aligns to Development and early Production phases (Figure 4-2).

4.4.1 Pre-Silicon Validation

Functional Unit/Cluster Level Simulation — Intel validation engineers test the internal workings of each major subsystem within the chip design with the goal of assuring each Functional Unit and Cluster functionally meets its specification. This validation is typically a software simulation in the design environment, where subsystem interfaces can be controlled and monitored. Software simulation enables a more targeted testing than is possible in hardware. With this approach, validation detects problems early and resolves them quickly to accelerate product development.

Chip Level Simulation — Chip level simulation tests the performance of all chip design subsystems operating simultaneously. All units are combined in an environment where stimulus is provided at the component pins. The primary focus is on unit and pin interfaces and global functionality. Interfaces are tightly controlled, and functionality is validated under an enormous variety of conditions.

System Level Simulation (SLS) — For system level simulation, the simulated component is tested in a full operating environment to ensure that it works with other platform components. Operation is also tested against industry bus standards to validate compatibility.

Emulation — Once a behavioral model for a chip is developed, it can be transformed to produce a hardware emulator. Emulation enables Intel engineers to validate the logic functionality of the design, to debug BIOS and software drivers, and to verify the quality of the tools and processes that will be used in post-silicon testing.

Intel is an industry leader in emulator technology application and has heavily invested in advanced hardware emulators to enable realistic pre-silicon validation. The advantage of hardware emulation is its speed, typically several orders of magnitude faster than software simulation. Each emulator can model tens of millions of gates at emulation frequencies exceeding 10 MHz. Another advantage is that it permits the behavioral model to run with actual external system hardware. Intel has also developed fast, proprietary interfaces to accelerate the testing process and enable a more comprehensive pre-silicon validation. All of these advantages are instrumental in improving overall quality and accelerating product development.

4.4.2 Post-Silicon Validation

System Validation — System Validation (SV) tests all the features and functions of a chip, as defined by its specifications, on a specialized, highly instrumented SV platform. Specialized SV hardware and software is designed to exercise all functions of the component, detect flaws, and facilitate root cause analysis. Testing paradigms include focused testing and directed random testing. Given its specialized nature, System Validation is tailored to the specific type of chip – either microprocessor or chipset.

Microprocessor — System Validation stresses both the architectural and micro-architectural features of the microprocessor, with a focus on cache coherency and multiprocessor environments. Systematic and random tests are used to cover very deep data space and intensive floating-point demands. System Validation tests for the Intel Pentium 4 processor offer an example of the scope and intensity of the process:

- 2,450 microprocessor feature tests; 2,000 legacy architectural tests
- 1 trillion random instructions tested per week
- Millions of chipset feature permutations and focused I/O stress testing

Chipset — All chipset features are tested with custom-built system validation boards and test cards. Performance parameters are pushed to their limits on cards and busses concurrently to validate performance limits and to verify bus compatibility.

For Intel chipsets that have integrated graphics, specialized tools and test suites are used for validation testing. Special test images are created to ensure a rigorous baseline for automated testing. Root cause is determined for every wrong bit so that the problem can be fully resolved, ensuring outstanding visual quality.

Analog Verification — Analog Validation focuses on processor and chipset signals to ensure functionality and specification compliance under varied environmental and voltage conditions. Component-level validation includes AC timings, buffer characteristics, and rise/fall times. Platform-level validation includes testing for signal integrity, power integrity, cross talk, and voltage droop.

Circuit Marginality Validation (CMV) — During Circuit Marginality Validation, test suites are applied to microprocessors that focus on reliability and performance under extreme operating conditions. Both commercial and custom tests are used to test at voltage, frequency, and temperature extremes, and to ensure reliable operations within the processor's specification.

Analog Integrity Engineering (AIE) — Analog Integrity Engineering tests the electrical integrity of the chipset to make sure the entire platform is electrically robust. Performance is validated under a wide variety of worst-case scenarios. Intel works closely with customers, providing simulation models, correlating models to silicon and validating electrical robustness to demanding test conditions.

Compatibility Validation (CV) — Compatibility Validation (CV) is performed on a complete, typical system that includes subsystems such as components, boards, chassis, BIOS, operating systems, and application software. Typical areas of CV coverage include:

- Functionality (application related requirements)
- Performance and benchmarking stress (concurrency, overloading)
- Conformance (standards, protocols)
- Interoperability/compatibility
- Usage models

4.4.3 Software Validation

Software validation tightly integrates with hardware validation to ensure that hardware and software components operate together smoothly. Successful software validation shows that the total platform delivers top performance and reliability in the widest possible range of real-world environments. Driver software validation begins during system-level emulation, well before manufacture of the first silicon prototypes of the new component. This accelerates hardware and software development by ensuring high quality drivers during early design stages.

All Intel software specified for use in a Microsoft® Windows operating environment undergoes Microsoft® Windows Hardware Quality Labs (WHQL) Certification testing. Intel executes proprietary tests in addition to the WHQL test suite to ensure exceptionally strong validation with Microsoft® applications and operating systems.

4.5 Product Transfer to Manufacturing

Together, qualification and validation enable robust physical, logical and electrical designs. To bring their benefits to market, the product must successfully transfer and ramp into manufacturing. Intel's Copy Exactly! procedure is key to successful product transfers (Section 6.2). It provides comprehensive set of evaluations, establishes critical process parameters, process capability and process control limits to enable transfer into manufacturing.

Intel Materials Quality organization acts as a conduit between Intel suppliers and Intel factories, Technology Development (TD) and product divisions. Intel Materials Quality uses a proven Quality Operating System (QOS) process to select, develop, and manage suppliers so that they are capable of delivering materials and services for high volume manufacturing. All incoming materials must meet the manufacturing requirements and must function as expected at the lowest total cost.

5. Materials Quality

The Material Quality Network (MQNW) consists of Materials Quality teams working with technology development, factories, and subcontractors in the factory supply chain. These teams play critical roles in all phases of the product life cycle, from product conception to product delivery. They work closely with suppliers to address issues that may occur, and drive supplier material and process improvements to meet manufacturing requirements. The net result is that production runs smoothly and the final product satisfies our customers. Figure 5-1 illustrates the interrelationships of the Material Quality Network and its relationship to the Material Life Cycle.

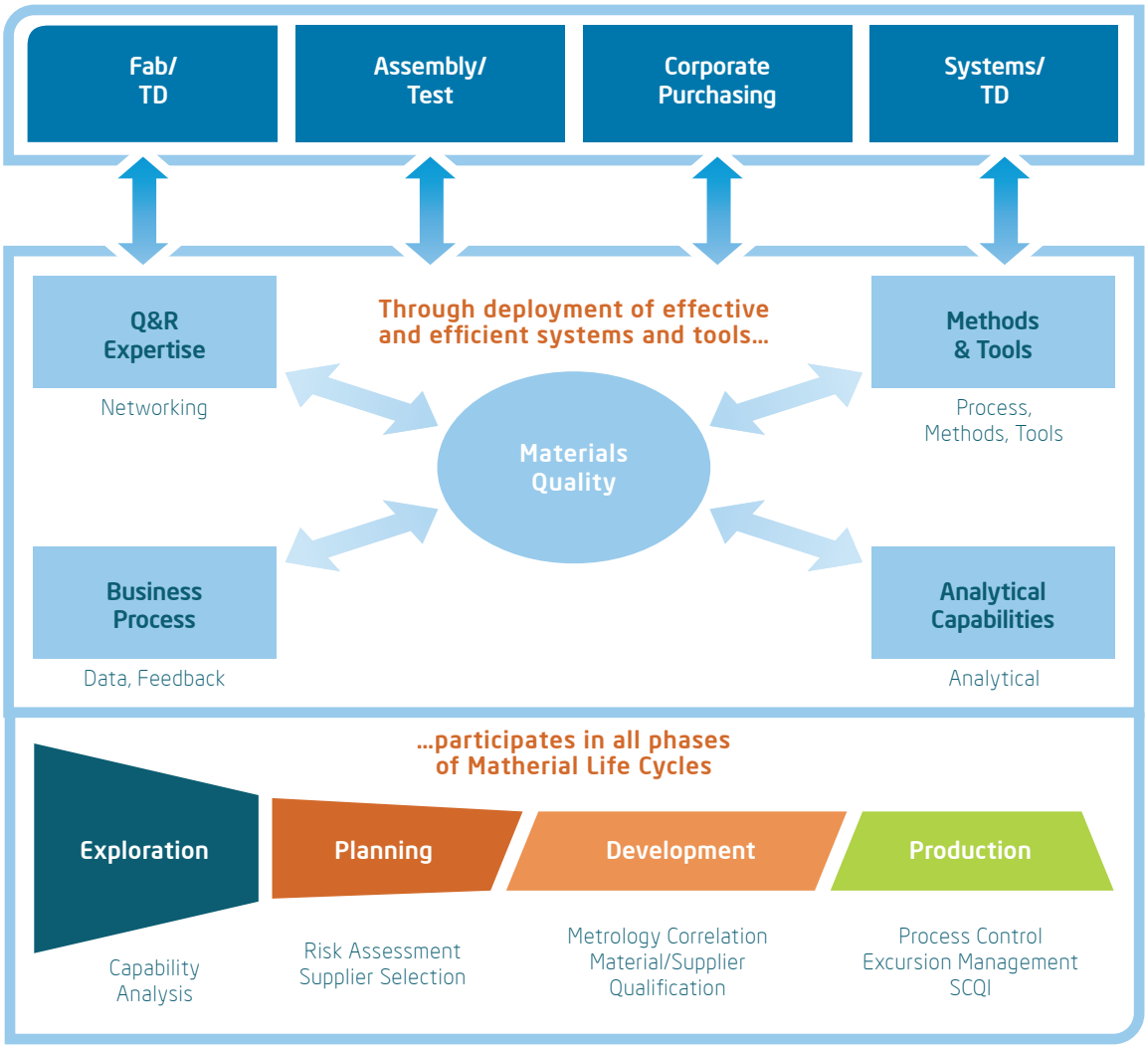


Figure 5-1: Materials Quality Network Interrelationships

5.1 Materials Quality System Platforms

The Materials Quality Operating System (QOS) is used to manage material and supplier quality. There are four platforms in the Materials QOS. Each platform has methods with associated tools, indicators, and training. Table 5-1 illustrates each of the four Materials QOS platforms and outcomes.

Key Materials Platform	Platform Outcome
Platform 1 - Supplier Selection/Development	Suppliers selected and developed with materials of the highest quality and lowest cost.
Platform 2 - Materials/ Supplier Qualification	High Volume Manufacturing (HVM) go/no-go decisions.
Platform 3 - Process Control System and Excursion Management	Change is controlled, with stable material quality and effective management of excursions.
Platform 4 - Supplier Continuous Quality Improvement	Improved supplier quality, overall capability, and costs.

Table 5-1: Key Materials QOS Platforms and Outcomes

5.1.1 Materials QOS Platform One - Supplier Selection

Each Materials group defines their requirements and assesses potential supplier candidates based on their capabilities. As part of their development, the selected supplier will receive appropriate training from Intel to close gaps in their systems in order for them to be successful in meeting business expectations. Figure 5-2 illustrates the steps involved in the supplier selection process.

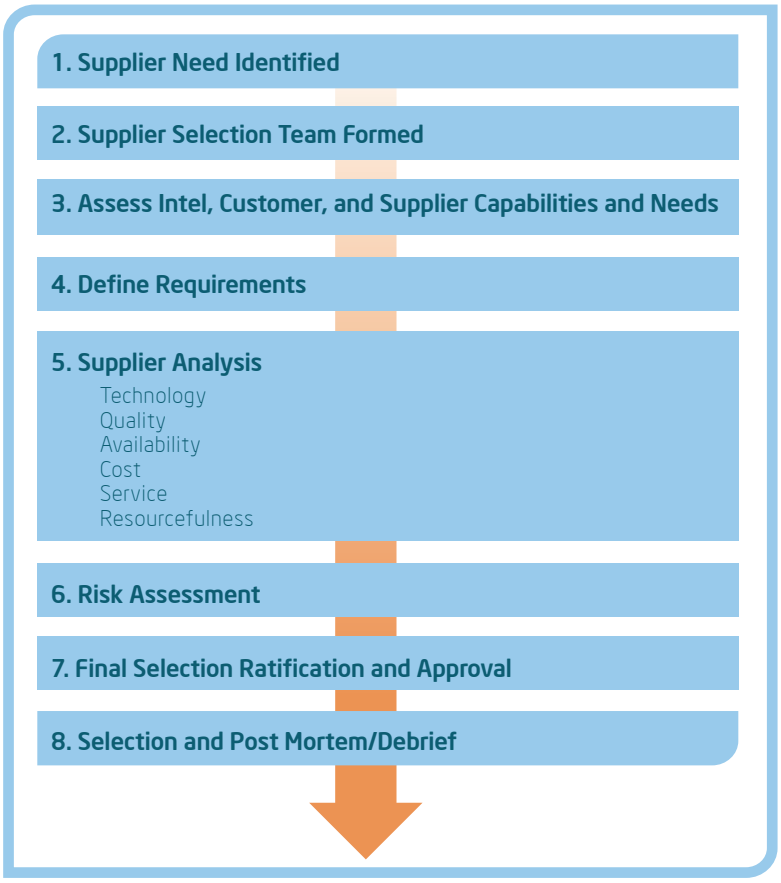


Figure 5-2 Supplier Selection Process Steps

5.1.2 Materials QOS Platform Two - Materials and Supplier Qualification

In this platform, the Materials group validates the capabilities of the supplier to support high volume manufacturing. Each Materials group establishes their business requirements and module target specifications (MTS).

Specific materials attributes must be satisfied to qualify a new material at Intel. They include quality and reliability requirements, specification requirements validation, and proven equivalence, if materials come from different suppliers or sites. New materials must also meet Intel manufacturing yield goals.

To qualify a new supplier at Intel, an effective supplier system must be in place. System expectations include change control, supplier quality reviews, valid sampling plans to enable incoming quality control elimination, reliability monitors, traceability, statistical process control with metrology, inspection correlation, and a corrective action system.

Intel uses Design of Experiments (DOE) audits to generate the data required for risk assessment and decision-making. Risk mitigation actions, such as ensuring materials quality, making process improvements, and requiring further training, may be necessary to prepare a supplier before final approval for production.

5.1.3 Materials QOS Platform Three - Supplier PCS and Excursion Management

In high volume manufacturing, the supplier must demonstrate the capability to maintain stable and predictable material quality and deal with any excursions in an effective manner. The purpose of Process Control System (PCS) and excursion management is to prevent excursions, and detect and react to them when they do occur to minimize any impact to the customer. Figure 5-3 categorizes the tools and processes Intel uses to control supplier processes and manage excursions.

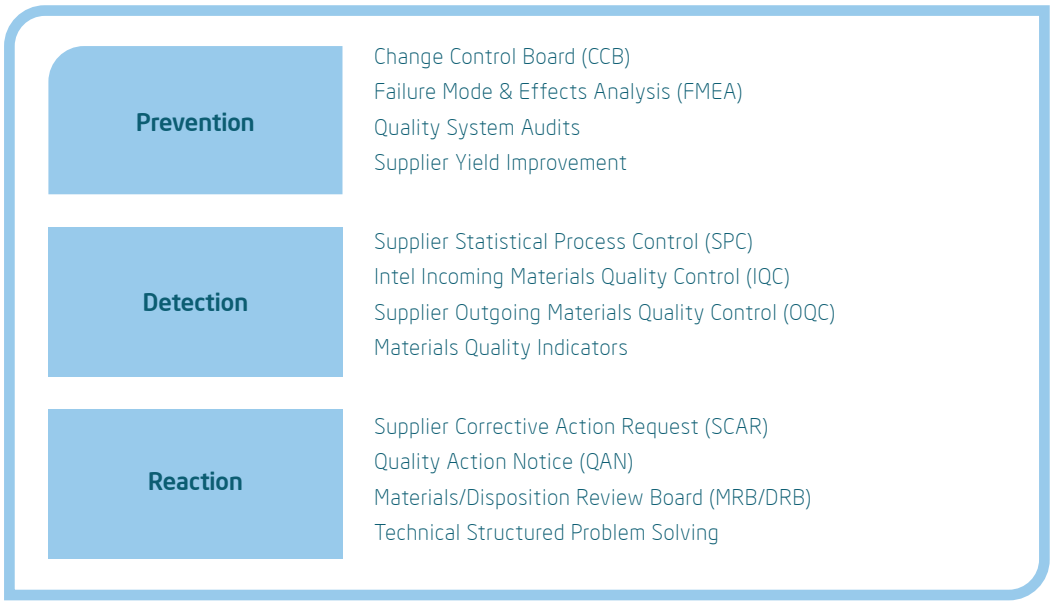


Figure 5-3: Elements of Process Control and Excursion Management

Prevention — Issue prevention tools reduce the occurrence of materials-related quality issues. Product and process change control prevent issues from arising due to unintended consequences of such changes. Tools such as Failure Mode and Effects Analysis can identify potential causes of issues and identify areas for preventive checks and balances. Quality system assessments identify areas for improvement, and supplier process yield improvements reduce the risk of non-conforming product or materials from being shipped. Intel's robust change control forum reviews and approves material and process changes and tracks the change results. Changes are limited and scheduled accordingly. This action controls the introduction of materials variation into the manufacturing system.

Detection — Process control methods are used to detect when materials-related quality issues occur. These methods include inspection tests, monitors and indicators that are designed to highlight when and where a quality issue arises. Early detection helps to prevent worsening or spread of the problem. Intel sets expectations for suppliers to have effective monitors to detect issues, and may include this expectation in the quality assessment agenda. Suppliers should provide updated control charts and timely closure for any out of control situation. Suppliers are rated on their process control maturity. If necessary, training may be provided to the supplier to reinforce their capability.

Reaction — Issue reaction includes the procedures used to contain and correct materials-related quality issues. These procedures notify the suppliers about quality issues and request corrective actions. They also address containment and disposition of questionable materials. Structured problem-solving methods determine the root cause and identify permanent corrective and preventive actions.

In the event of an excursion, Intel expects suppliers to trace discrepant materials and isolate them. Risk assessment must be performed, and the materials must be disposed appropriately, based on the technical and business implications. The root cause of the problem must be determined and fixed within a specified time frame to avoid manufacturing and customer impacts.

5.1.4 Materials QOS Platform Four - Supplier Continuous Improvement

The purpose of this platform is to improve the performance of Intel suppliers. The supplier's performance is assessed in several areas, including quality and opportunities for improvement. The Materials group and the supplier jointly coordinate supplier improvement activities. The tools used in this platform include:

- **Supplier Scorecard** — to rate the supplier in critical categories, such as cost, quality, availability, technology and customer satisfaction
- **Supplier Standardized Quality Assessment (SSQA)** — conducted jointly by Intel and a supplier to identify areas of strength and system improvement opportunities
- **Annual Improvement Plan (AIP)** — to identify specific areas that Intel and supplier work together on selected activities and key results
- **Supplier Business Review (SBR) —** meetings to communicate performance, progress, and outcome of selected activities in the Annual Improvement Plan
- **Supplier Corrective Action Request (SCAR) —** to alert the supplier of a serious issue requiring immediate action. The supplier is expected to report their findings and commit to closing the issue in a timely manner

The Supplier Continuous Quality Improvement Cycle illustrates how Intel and the supplier work together on quality improvement (Figure 5-4).

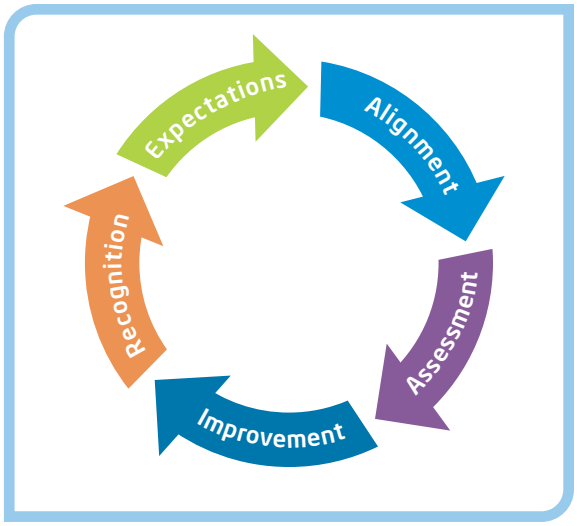


Figure 5-4: Supplier Continuous Quality Improvement Cycle

Intel and the supplier discuss their expectations and then align activities and indicators. Expectations, activities, and indicators are tracked and assessed periodically so that improvements can be made in identified areas.

When suppliers excel in specific areas and their overall scorecard performance, Intel may recognize their accomplishments in an appropriate forum.

5.1.5 Supplier Continuous Quality Improvement Program

The Supplier Continuous Quality Improvement Program (SCQI) directs, monitors, and rewards supplier-driven quality improvement. Suppliers that excel in this area receive public recognition from Intel.

The SCQI vision establishes relationships with a select group of key suppliers who provide the highest quality materials, equipment, and services with a commitment to continuous improvement. To enable this vision:

- Intel and the supplier mutually drive continuous improvements
- Key or strategic suppliers are placed on the SCQI roadmap and certified
- The SCQI program is viewed as a journey toward operational excellence rather than a destination

Intel and the supplier mutually establish goals and expectations and commit to allocate time and resources to participate in this program. Supplier performance is tracked in report cards that contain evaluations of a supplier's performance against expectations with input from Intel managers, Intel Quality and Reliability, and the Intel factories. Routine quality assessments are conducted to identify areas for improvement in the supplier's quality systems. Supplier improvement plans are generated jointly between Intel and the supplier's management to address the gaps identified in the supplier assessments and the supplier report cards.

Supplier Awards — Suppliers Awards are part of the SCQI program. It recognizes suppliers who exhibit excellence in their assessment scores, report cards, and performance in their improvement plans receive recognition from Intel. Figure 5-5 illustrates the progressive recognition of supplier awards. Performance is recognized by one of three performance awards:

- **Certified Supplier Award Certification** — awarded to suppliers consistently meeting Intel expectations. Suppliers have achieved 80% scores in their report cards for 2 quarters with no major issues in SSQA.
- **Preferred Quality Supplier** — awarded to suppliers consistently exceeding Intel expectations. Suppliers have achieved better than 80% scores on their report cards for a year, with no major issues in SSQ. Their superior quality systems provide consistent and predictable performance.
- **Supplier Quality Improvement Award (SCQI)** — awarded to suppliers who have achieved better than 95% scores on their report cards for a year. They are the best in their class and have shown consistent, predictable performance that outpaces other suppliers. They are industry role models for their products, services, and business practices.



Figure 5-5: Supplier Awards Progression

5.2 Metrology Labs

The Metrology Lab characterizes new materials and develops metrology equipment and methods to monitor critical parameters. To ensure that metrology is never a gating factor at product launch, Materials Quality requires in-process metrics and end-of-line metrics at major assembly materials suppliers and assembly subcontractors.

The critical steps in the metrology development and deployment require the Metrology Labs to work closely with the suppliers. Their objectives are to a) define quality metrics, b) develop the metrology capability, c) characterize materials, d) proliferate this new capability to the suppliers, and e) and assure suppliers incorporate the metrics into their process control systems. Once Intel and supplier metrologies correlate, the supplier's process control data is accepted and the materials are placed in a "No Inspection Necessary" or "Dock to Stock" status.

5.3 Subcontractor/Outsourcing Quality

Intel uses subcontractors to perform some or all of the manufacturing process steps, including wafer production, assembly, test, board, and system manufacturing. Potential subcontractors are evaluated on their ability to meet technical, business, and quality requirements. Only suppliers that measure up to Intel form, fit, and function specifications are certified to manufacture products bearing the Intel logo. Intel is able to offer customers a wider choice of products and increase the availability of some products because certification of subcontractors results in overall customer support improvement while meeting Intel's high standards of product performance and quality.

Once a subcontractor site is certified and products are qualified, subcontractor quality management is similar to other supplier management. Intel's Material Quality System resembles a standard supplier management system:

- Quality monitors are required to produce a reliable indication of shipped quality
- Process changes are subject to approval via Intel's change management process
- Excursion response is closely managed
- Improvement areas are identified through regular quality process audits and quality system
- Supplier Business Reviews and a scorecard process assure good communication and alignment on trends and requirements

6. Manufacturing Quality Systems

The Manufacturing Quality System encompasses Intel products from silicon and components to boards and modules. To deliver products efficiently that meet Intel's customer expectations, Manufacturing transfers proven quality system fundamentals into each new business area. Issue prevention is the focus, utilizing systems that enable the prevention, detection, and containment of issues. Validation through assessments and audits focuses on business processes and quality culture. The best-known methods captured through these assessments are shared across factories.

6.1 Factory Overview

Intel's manufacturing organization encompasses wafer fabrication, assembly, high-volume testing, boards manufacturing, and outsourcing. This geographically dispersed manufacturing organization consists of:

- Wafer fabrication facilities in eight U.S. sites, and sites in Ireland and Israel
- Assembly and manufacturing test facilities in the United States, Malaysia, Costa Rica, China, and the Philippines
- Subcontracting and outsourcing facilities in multiple worldwide locations

At each manufacturing site, the Quality and Reliability staff monitors quality, provides feedback to the Product Design and Technology Development organizations, and participates in problem solving. The local quality and reliability organizations report jointly to local site management and the Corporate Quality Network management, thus meeting local needs and maintaining policy consistency across Intel.

Internal training organizations develop and provide training for manufacturing job functions, including supervisors, engineers, and factory support personnel. All manufacturing technicians and production operators receive training for their job and certification to a set of competencies. Each factory has a training group that is responsible for developing manufacturing skills specific to its needs. Intel emphasizes training in statistics, Statistical Process Control, structured problem solving, and team building.

The local organizations have the responsibility and authority to improve product quality and reliability through the following actions:

- Identify and record problems and corrective actions
- Initiate and provide solutions and improvements
- Verify implementation of solutions
- Control nonconforming products until deficiencies are corrected
- Initiate actions to prevent nonconformities
- Share information and best-known methods across the geographically dispersed organizations

6.2 Environmental Citizenship

Over the past several years, environmental focus has expanded from the manufacturing of electronic products to the environmental attributes of the electronic products themselves. This expanded focus presents an interesting challenge for the highly specialized and distributed world of electronics manufacturing.

Intel has long focused on design for the environment and improving its environmental performance. However, this focus has historically been at the manufacturing level. That is, reducing and minimizing the environmental impact of its manufacturing processes as each new generation of microprocessor is introduced. As environmental attention has turned to the performance of electronic products, Intel has expanded its own environmental focus to include the environmental attributes of the components it produces.

Although our components make up a small piece of the final electronic device sold to the consumer, we believe that our role can be significant in helping to minimize the environmental impact of the final product.

As a company, we are committed to conserving natural resources, reducing environmental impact and developing environmentally compatible products and processes.

Intel's Corporate Responsibility Report (http://intel.com/intel/finance/gcr05/index.htm) and the Intel Environmental Health and Safety Policy (http://www.intel.com/intel/other/ehs/policy.htm) describe Intel's policy, goals, and progress to reduce and minimize the environmental impact of Intel products.

6.3 Copy Exactly!

Fab, Sort and Assembly Test Manufacturing follow a Copy Exactly (CE!) philosophy. Copy Exactly! enables delivery of product from multiple production sites, which operate as a virtual factory that performs consistently and independent of the manufacturing source site. Additional benefits include faster production ramps that improve product availability and improved consistency to quality performance. Intel found that copying the embedded learning from the development Fab was the key to minimizing output loss with process transfer. This led to the development of the Intel Copy Exactly! Method (Figure 6-1).

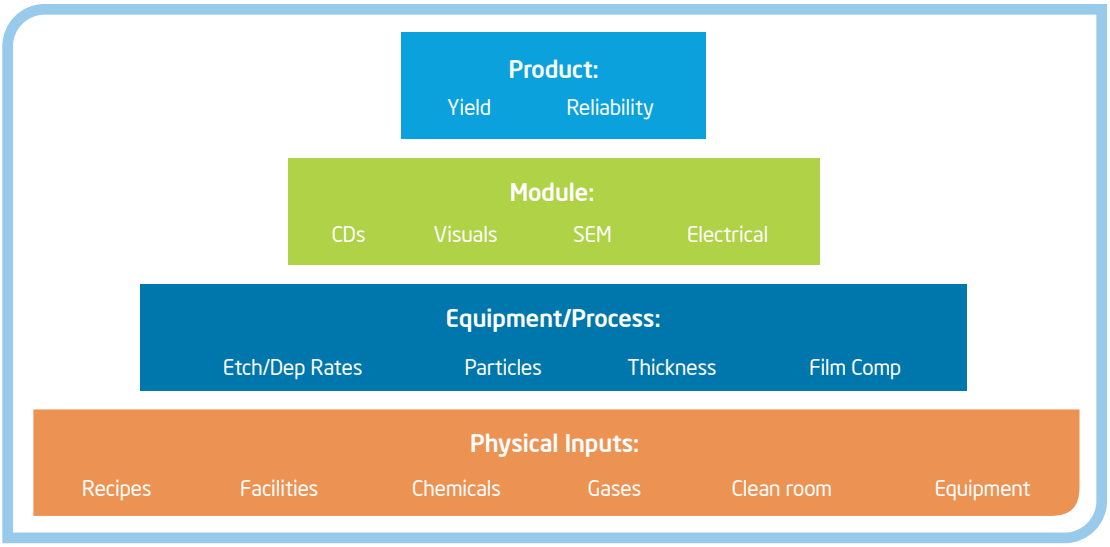


Figure 6-1: Copy Exactly! Methodology

The Copy Exactly! Methodology focuses on matching the manufacturing site to the development site. Matching occurs at all levels for physical inputs and statistically matched responses (outputs). This process enables continuous matching over time by using coordinated changes, audits, process control systems, and joint Fab management structures.

Physical inputs such as equipment configuration, chemical purity, facilities, and equipment hookups derive from the same specifications. In-line process or equipment monitors that predict product performance, yield, or reliability must match at all levels.

Early in the transfer, Process Technology Development (Process TD) selects process and product parameters for statistical control and documents detailed control plans. Process TD continues working with the factory location to achieve process control and yield targets in high volume manufacturing. Throughout the transfer, factory personnel are responsible for quality and statistical control of all key parameters.

Once matched, changes are coordinated through joint engineering teams. Intel performs cross-site audits of equipment configuration and in-line process and equipment monitor results using a common process control system. Fabs execute high-level tactical and strategic changes under the auspices of the joint engineering and strategic management structure. As each factory begins to build a new technology, it starts at the same yield and improves at the same rate as the other factories.

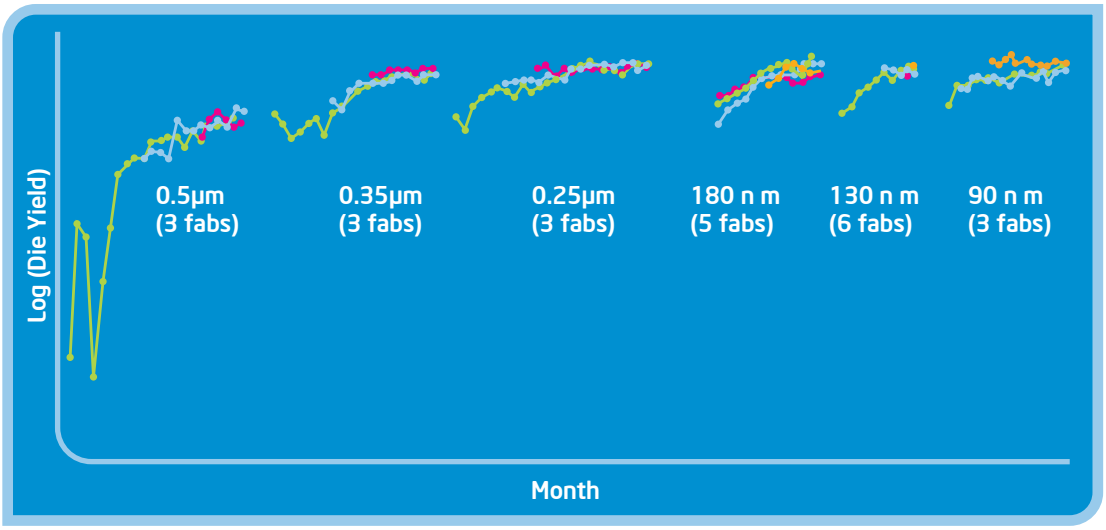


Figure 6-2: Results of Copy Exactly! Methodology

6.3.1 Process Change Management

The Process Change Control Board (PCCB) is the primary tool for control and managing process changes in Intel factories. The PCCB process requires that appropriate technical forums review changes, stakeholder notification, and that qualification plans and success criteria are documented in a PCCB white paper. Additionally, the process addresses technical and practical concerns raised by key stakeholders, and verifies that:

- Changes are documented
- Changes are value-add
- Proposed implementation plans are comprehensive, timely, and realistic
- Anticipated risks are addressed
- The factory is committed to the implementation of the change as documented in a white paper
- Benefits are verified following implementation
- Assigned tasks are tracked through completion

6.4 Manufacturing Systems

6.4.1 Factory Process Control

Statistical Process Control (SPC) tools allow Intel Manufacturing to identify problems early and prevent excursions. Station-manufacturing SPC is a key tool to reduce variability of key parameters for all of the manufacturing and job processes/products.

In-line process control monitoring is ongoing, and significant parameters are tracked using tools such as control charts. The goal is to monitor any parameter that may affect the final product's performance or factory flow. Every process step has a number of monitored variables. For example, in a bonding operation the monitored parameters may include machine controls (e.g., power, pressure, time, frequency) and finished product parameters (e.g., bond pulls and thermal cycling performance). For a photo resist development step, these variables might be equipment-related (e.g., develop volume, water pressure, spin speed) and inspections-related (e.g., amount of residual resist, levels of contamination).

As processes, equipment, and products change, the monitoring program and parameters evolve. Ongoing learnings change the way Intel monitors its Fab, assembly, and board processes. A monitor may be eliminated or replaced with a more effective one if it is no longer generating useful information. At other times, monitors may be added to address problems until implementation of corrective actions.

Station-manufacturing statistical process control is performed with a real-time, computer-based capability. Real-time operator inspections and key parameters monitoring allow immediate corrective action when process drifts occur. Manufacturing technicians and engineers use response flow checklists and decision trees to address process interruptions and significant out-of-statistical-control indications.

Intel monitors the health and effectiveness of the process control systems by examining various metrics such as control chart run rates, centering metrics, control limit health, and tool matching metrics.

6.4.2 Continuously Improvement of Products and Services

Manufacturing engineers continually focus on defect reduction and process margin improvement. Technical structured problem solving methods are taught and used extensively. These common methods allow cross-functional teams to form quickly, to address improvement opportunities with a common approach and language, and to focus on root cause and systemic corrective actions. Problem solving methods and tools such as Pareto analysis, process flow charts, and cause-effect diagrams are widely used. Advanced statistical methods such as response surface analysis and statistical experimental design are used to pinpoint the root cause of process variations or other manufacturing issues. Site statisticians assist teams and individuals in using statistical methods.

Intel manufacturing systems integrate advanced statistical methods with other types of data systems to produce powerful and effective improvement tools. One example is the integration of test information across individual wafers with data from the process control system. This allows for statistical correlation of wafer Fab process parameters with device yield and performance data at the individual die level. The resulting wafer map studies have proven to be a valuable tool for finding and reducing sources of variation and yield loss. For additional information, refer to "Reliability Improvement and Burn In Optimization Through the Use of Die Level Predictive Modeling" and "Unit Level Predicted Yield: A Method of Die Level Defect Reliability Segregation" proceedings. See References Section for additional details.

New wafer Fab equipment qualification begins in the strategic capabilities and technology development organizations. There, the manufacturer's specifications are validated and a manufacturability evaluation is performed. Upon meeting requirements, it is transferred for beta site testing in a production area. Beta test criteria are tailored to the process step involved. Procedures are similar for qualifying new equipment or adding equipment to installed base. Copy Exactly! Methodologies are also applied for establishing machine control limits, in-line control

criteria and finished product performance criteria such as yields and reliability. The process includes an exhaustive fingerprinting to enable the added equipment behaves like the existing equipment. This includes matching physical inputs such as gas flows, plumbing, and matching product and performance parameters. Process module (several sequential manufacturing steps) testing is also performed to check for interactions with the installed equipment base.

Change Control Boards review all equipment qualification plan changes. These boards require the use of rigorous statistical methods, including sequential matching for equipment qualifications. Once in the production environment, equipment undergoes preventive maintenance monitoring with a predetermined frequency. Preventive maintenance specifications provide the details including PM frequency and equipment maintenance logging requirements.

6.4.3 Monitors and Manufacturing Quality Audits

Reliability Screens, Monitors and Sampling — Product and process reliability monitors are defined and used in various stages of product development and qualification. They are executed in-line or off-line as needed in wafer fabrication, assembly, boards and systems processes. Some monitors are defined during development and are continued into the manufacturing life of a product.

In addition to monitors, certain reliability screens are included in wafer-sort testing or finished product testing. Examples include margin screens, such as guard-banding charge-loss performance on memory cells, and defect screens such as high-voltage cell stress for gate dielectrics.

Intel performs periodic sample monitoring for each wafer Fab, assembly, board, and package assembly process. The sample size criteria varies based on process attributes. For example, package reliability monitors consider such factors as high sensitivity to reliability stress, cavity type, frame type, lead count, and die attach method. Sampling plans also consider production volumes and failure analysis complexity.

Each sampling plan has defined control limits and reaction plans. The reaction plans include quickly validating failures, identifying their potential impact on product reliability, and determining corrective actions. Quality and reliability engineering teams routinely review these indicators and drive appropriate actions and responses to make sure that they are healthy.

Internal Quality System Audits — Internal auditing determines if requirements are met, evaluates processes and systems for effectiveness and efficiency, and identifies opportunities for continual improvement. The ISO 9001 standard serves as the baseline for quality system requirements throughout Intel's worldwide factory and outsource network.

Each manufacturing site has a Lead Assessor responsible for the Internal Quality Audit System. The Lead Assessor coordinates all internal audit activities including managing the audit team; team members are from different aspects of Manufacturing and support groups and are highly trained in audit skills.

Each member of the audit team shows a high degree of independence and is not assigned duties or engages in activities that would interfere with auditing.

The Lead Assessor develops audit plans for their manufacturing site. Manufacturing reviews and update these plans quarterly based on business needs and risks. Upon audit completion, the Lead Assessor provides the factory staff with an assessment of the adequacy and effectiveness of the systems and processes in use. If necessary, the factory staff or the area owner recommends improvements or corrective actions to the existing systems and operations. A system-wide corrective action tracking system monitors actions for closure. Corrective actions are verified to make certain that they become permanent.

Self-Audits — Self-audits are another method Intel uses to monitor systems. Self-audits are in-depth assessments led by a processes owner or expert. Self-audit teams, composed of functional content experts, train on basic auditing methods and techniques and ISO 9001 requirements. Self-audits include planning and performing the audit, reporting the audit findings, tracking corrective action closure and effectiveness, and continuous improvement planning. At a minimum, sites and operations perform annual self-audits of their quality system and processes. Regularly scheduled management reviews monitor corrective action closure and the overall effectiveness of the program.

6.4.4 Factory Environmental Control

Intel factories control environmental factors such as air purity, humidity, temperature, and electro-static charge where needed for comfort, contamination control, and process optimization.

Cleanroom air is filtered to achieve Class 1 conditions in the process areas. The velocity and directional of airflow is also controlled in the process area, and cleanrooms are maintained in positive pressure relative to the outside environment. Intel factories control relative humidity to accommodate operator comfort, reduce electrostatic charge, and chemical processes optimization. Factories control ambient temperature for operator comfort and as required by sensitive equipment. Since the motion of air, people, and equipment contribute to the generation of electrostatic charge, ceiling ionizers are used for static mitigation. The ionizers neutralize any generated charge before discharge can occur, and thus help prevent damage to circuits during the production process.

6.5 Control of Inspection, Measuring and Test Equipment

Intel's calibration program ensures the measurement capability of any instrument that provides quantitative or qualitative data on Intel products. The program includes mechanical, electrical, electronic, and physical measurements. Its purpose is to meet ISO 9001 and customer requirements and maintain traceability to national standards. Intel's Measuring Equipment and Calibration Policy require all inspection and test equipment used in the manufacturing environment or for product acceptance to be under calibration control at all times.

The calibration service ensures that all measuring and test equipment meets the specified tolerances. The calibration process corrects and compensates for drift, inaccuracies, and out-of-tolerance conditions found in equipment. Notification is required if an out-of-tolerance condition is found. Reports of calibration results are available at the certifying facility.

A network of laboratories located at major Intel sites worldwide provides the calibration service to maintain cost-effective, accurate measurements. This network maintains or has access to primary and secondary standards for voltage, current, resistance, frequency, mass, light intensity, dimensional parameters and others. Each site tracks equipment to verify and schedule calibration and maintain calibration traceability. Equipment owners are responsible for ensuring equipment calibration and each department is responsible for conformance to the calibration policy.

A system of standards and procedures helps enable product uniformity across manufacturing sites while internal audits achieve monitoring and compliance. Uniform application of the calibration system and development of calibration policies and practices are the responsibility of the Standards Labs.

6.5.1 Calibration Traceability

A traceability process links inspection and test instruments through Intel standards laboratories to the National Institute of Standards and Technology (NIST), acceptable international standards, or natural physical constants (Figure 6-3). Where no recognized national standard is available, consensus standards are used. These can include an artifact or process used as a de facto standard by agreement of the contractor.

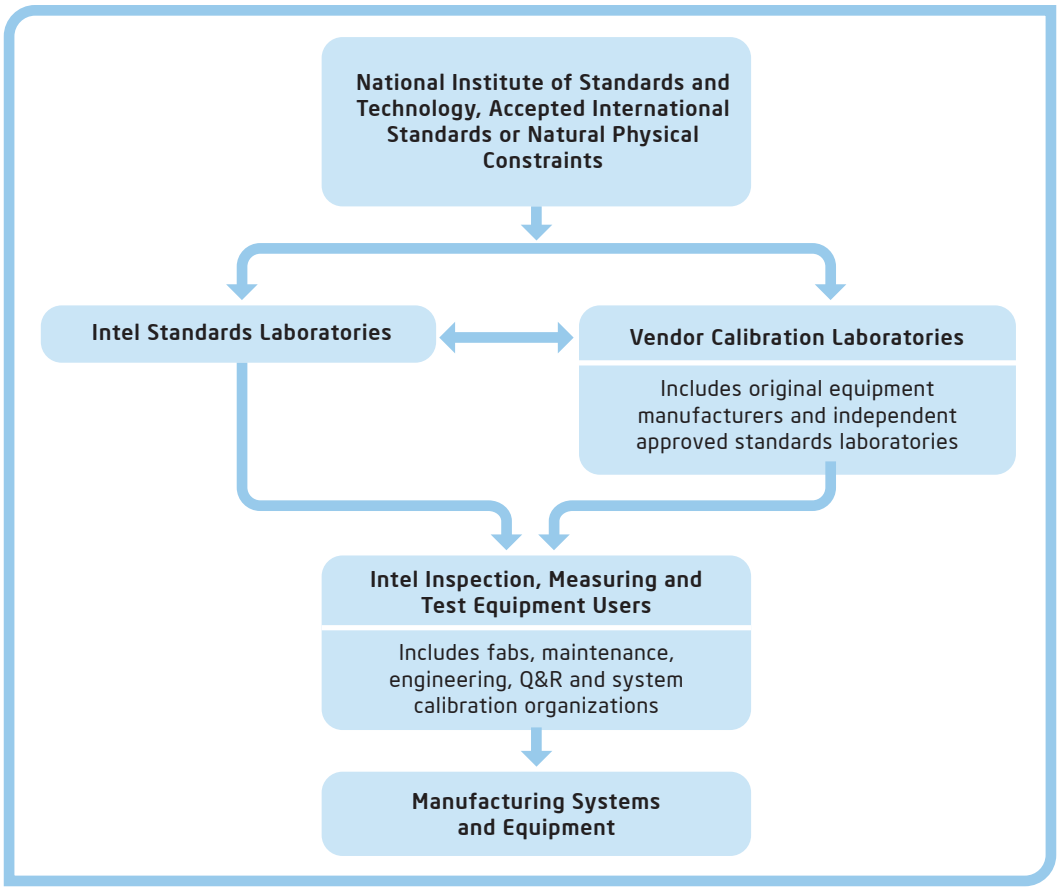


Figure 6-3: Calibration Traceability Chain

6.5.2 Calibration Capability

Intel tailors measurement requirements for calibration facilities to meet the specifications of each site. There are many different testing requirements and each calibration facility has a range of standards designed to the equipment owner's needs. At a location where a calibration capability does not exist, another Intel location or a vendor calibration laboratory may perform calibrations.

6.5.3 Calibration Intervals and Records

Intel establishes initial calibration intervals for measuring equipment and measurement standards based on manufacturer recommendations or local site Standards Lab operating procedures. After obtaining a sufficient history of the stability, calibration intervals can be extended based on risk analysis or shortened to enable equipment reliability.

Calibration labels identify unique tracking systems, the present calibration status, and the individual support group. They serve as a visible indicator of unit serviceability. Some labels are valid only when sealed with the appropriate site calibration stamp by a qualified Standards Lab team member.

The calibration system requires the following data and equipment maintenance information in a calibration record:

- Unique identification of unit tested
- Environmental condition under which the unit is tested
- Deviations, correction factors or limits of calibration, if applicable
- Equipment owner/user department
- Calibration interval
- Last calibration date and next due date
- Calibration procedures
- Repair information, if applicable
- Identity of person performing the calibration
- Standards used to perform the calibration

6.6 Control of Nonconforming Product

A corporate specification governs the review and disposition of questionable or discrepant nonconforming product across Intel, including wafer fabs, assembly and test sites, distribution centers, and business divisions. The specification details the requirements for review and disposition of nonconforming product or raw materials.

Operational procedures are also used to define detailed disposition procedures, including scrap, rework, or release criteria. All nonconforming products are subject to a formal risk assessment of potential performance degradation by a Disposition Review Board (DRB), Material Review Board (MRB), or Quality Action Notice (QAN).

Review board membership varies by site, product, or problem situation. Membership may include representatives from manufacturing, engineering, quality and reliability, and planning and other business and technical resources as needed.

The process begins when discrepant material is identified. The review board process will then:

- Identify and quarantine affected material
- Conduct a risk assessment and develop a material evaluation plan

- Identify the root cause
- Develop a corrective/preventive action plan
- Implement the corrective/preventive action plan
- Disposition affected material

Actions are tracked to successful conclusion and the review board creates a final report to document all actions taken to disposition the affected material. The board ensures that all preventive actions are completed or transferred to an organization/owner and monitored to assure the permanent solution is effective. The reports are used as reference for future excursion management and problem resolution. Additionally, factory self-audits, corporate audits, and quality system audits help define needed improvements.

6.7 Product Identification and Traceability

Intel employs systems to manage Product Identification with Unit Level Traceability for CPUs and Chipsets and Lot Level Traceability for Boards and Systems. A Record Retention System is used to manage and store this information.

6.7.1 Latest Generation CPU and Chipset Product Identification

Intel's component traceability system enables product identification and tracking through all stages of manufacturing, storage, and shipment to the first point of sale. Identification methods include lot-tracking numbers that allow forward and reverse traceability of products. Periodic audits are performed at each site to ensure compliance. Record retention guidelines ensure lot history maintenance.

Intel moves component production material through the factories in lots. For component products, Intel assigns a unique Fab lot number. When Assembly receives the released lots, an Assembly Lot Traveler is assigned to track the lot through the Assembly operations. At selected locations throughout the Assembly/Test and Finish processes, each unit is identified through the 2-D mark establishing unit level traceability, with critical data associated with these individual units.

6.7.2 Boards and Systems Product Identification

Production materials move through the factories in work order lots, which assign a unique serial number to individual boards. This serial number is the key identifier linking the board or system to a particular lot and its manufacturing history, including components mounted on the board or system, and shipment destination records.

6.7.3 Records Retention/Retrieval

Intel's Records Management Policy requires keeping records pertaining to product traceability for up to seven years unless mandated otherwise.

In components manufacturing the tracking system provides lot and unit genealogy, last known location, and status of products. This system facilitates tracing component products from the customer back to the Fab lot and from the Fab lot to the customer/location. Figure 6-4 shows how data feeds into databases and moves to the tracking system.

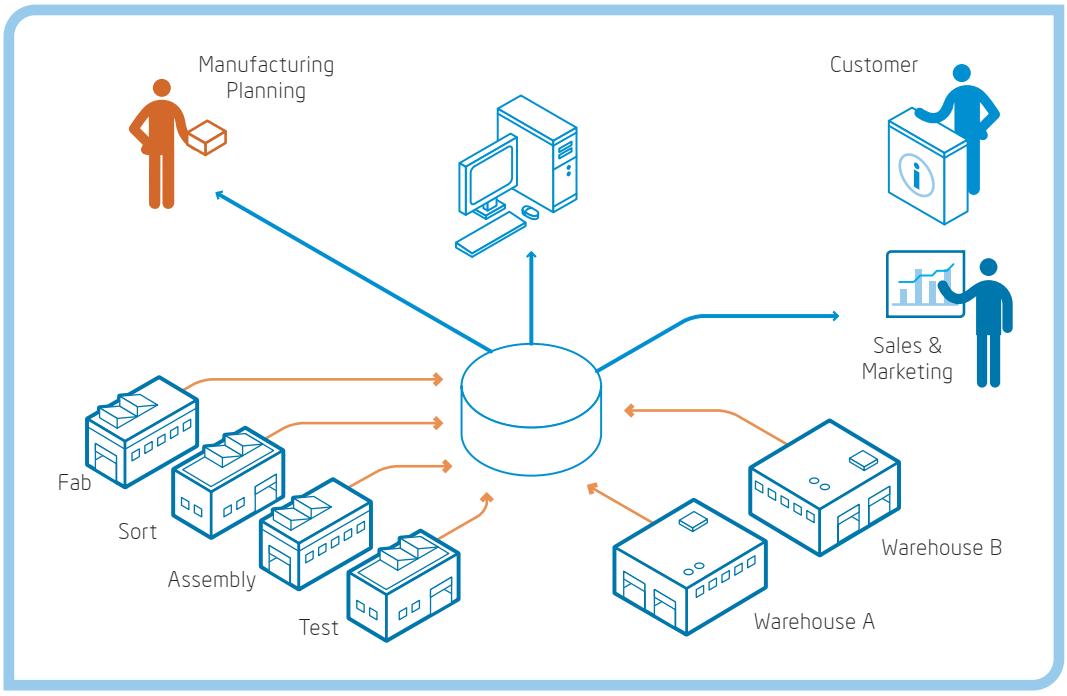


Figure 6-4: Inventory Management System

7. Customer Support

Intel has an extensive Customer Quality Support Network and processes that support technical and order fulfillment quality issue resolution, return materials authorizations, launch coordination and collaboration. Change Management and the Customer Excellence Program are also important parts of the Customer Support process.

Intel's Customer Quality Support Network mission is to provide best-in-class quality support services to our customers, offer value-added services for technical problem solving, enable timely launch of new Intel technologies and products in our customers' production, enable robust manufacturing, and create an environment where leadership, innovation, and impact are rewarded.

The Customer Quality Support Network responsibilities include:

- Understanding Intel customer quality and reliability requirements and product expectations
- Resolving customer usability and quality issues
- Recommending standard and uniform internal quality goals based on customer expectations
- Enabling customer manufacturing launch of new Intel technologies through specialized services
- Measuring customer satisfaction as part of the Intel Customer Excellence Program

7.1 Support Network Operations

There are a number of ways for customers to engage Intel for support. The worldwide internet access includes multiple language support and can be found at http://support.intel.com. Many types of support information and Intel's customer Support Hotline phone numbers can be found there. Customers in North America can call 1-800-628-8686.

Some direct purchase customers (those who buy product directly from Intel) have a dedicated account team. These teams include Field Sales Engineers (FSE) and Field Applications Engineers (FAE) who are focal points for the customer during the early design and pre-launch stages. The teams also include Customer Quality Engineers (CQE) and Corporate Business Analysts (CBA) who serve as the primary contacts for technical quality and order fulfillment concerns after product launch.

Direct customers have the option of contacting their account teams or Intel's Customer Support Hotline to resolve any technical issues arising from use of Intel products. Intel Channel Customers (those who buy product through authorized Intel Distributors), have the option of calling Intel's Customer Support Hotline.

7.2 Customer Quality Support and Services

Intel's Customer Quality Support Network offers a broad portfolio of technical, enabling, and support services and programs:

- Materials declaration data sheet
- Manufacturing enabling
- Product change management
- Order fulfillment quality
- Technical quality
- Returns management
- Customer Excellence Program

For Intel customers, effective use of these systems can lower the cost of doing business, speed time-to-market, and increase competitiveness. These systems are designed to help Intel understand customer needs and to furnish customers with valuable information about Intel products and services.

7.2.1 Material Declaration Data Sheets

Intel uses Materials Declaration Data Sheets (MDDS), which provide the necessary material composition information on restricted and banned substances. Intel's MDDS is based on a format established by the Electronic Industries Alliance, the European Information and Communication Technology Association, and the Japan Green Procurement Survey Standardization Initiative. This industry standard format is published as the Joint Industry Guide for Material Composition Declaration and can be accessed at http://www.eia.org/new_policy/jig_download.phtml.

Materials Declaration Data Sheets for most Intel components are available on the internet at http://developer.intel.com/design/packtech/packbook.htm in the section titled "Material Content of IC Packaging." This web site also contains an introduction with additional information on the industry's chemical content reporting requirements and Intel's chemical content reporting process.

7.2.2 Manufacturing Enabling

Intel's Manufacturing Enabling program supports new product technology introduction at our customers' sites. Successful launches result in higher yields and improved quality and reliability. Through this program, Intel develops and deploys technical training collaterals to communicate manufacturing best-known methods, best-known practices, practical handling, and installation tips. These collaterals accelerate customer leaning and skills to help them more quickly ramp up new technologies in their factories. For more information, see http://www.intel.com/design/reliability/index.htm.

7.2.3 Product Change Management

Product changes result from a variety of reasons including adding manufacturing capacity, yield improvements, quality improvements, supplier changes, and customer requests. Product Change Management is the process used to control the modification to a product's performance, appearance, quality, reliability, interchangeability, functionality, usability, supportability, manufacturability, customer handling, ability to integrate, and software interface. Intel's minimum guidelines follow the industry standards set fourth in the JESD46-B and JESD48-A for Product Change Notifications and Product Discontinuances respectively. Although Intel uses these standards as guidelines, we handle exceptions on an as-needed basis.

Customer Change Notification — Communicating changes to customers and ensuring their readiness to receive enhanced product are key elements of Intel's change management system. The objectives of the change notification system are to:

- Communicate critical information, including expected customer impact
- Provide sufficient evaluation time
- Enable fast and controlled factory changes, product enhancements, and process improvements

The Communication and Notification Flow (Figure 7-1) shows the progress of conversions from change inception through customer notification and factory implementation. Customer Notification Change Forums (CNCF) track conversions from initiation through implementation.

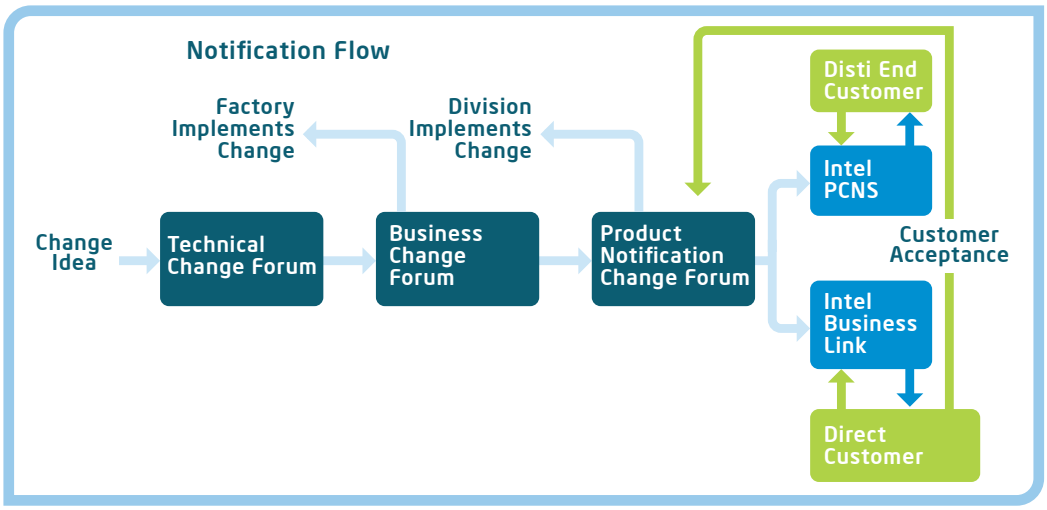


Figure 7-1: Communication and Notification Flow

Notification Criteria — The Product Change Notification (PCN) is the primary mechanism used to communicate product changes to Intel customers. Intel's notification criteria apply to any products that have reached Product Release Qualification (Chapter 4) and are sold for revenue. Upon receiving a PCN, customers should to evaluate the impact of the change on their products and factory operations.

The information included in a PCN typically includes:

- conversion number
- conversion title
- type of change
- type of notification
- customer acceptance deadline
- recommended action for customer
- description/reason for change
- milestone dates
- products affected
- products discontinued
- order codes affected
- reference documents

Key Characteristic of Change — Intel categorizes all changes according to a list of key characteristics. Product Design and Manufacturing site key characteristics of change affect the form, fit, function or reliability of the product. A change in form, fit, function or reliability may have significant impact on a customers application (e.g. electrical or performance characteristics) or on a customer's manufacturing process. These changes may or may not exceed product data sheet parameters. Qualification samples are typically available to direct customers 60 days before the customer must be ready to receive the new material. Qualification data is made available before the conversion date.

A list of all the key characteristics of change along with their definition is listed below.

a) **Product Discontinuance** — Intel provides product discontinuance notifications to direct customers and authorized distributors, allowing customers to place final purchase orders. Customers are notified if they are in the design phase or have purchased product from Intel within the last two rolling years before the product discontinuance notification. Intel-authorized distributors are required to provide product discontinuance notifications to their end customer(s) who have purchased Intel product from the distribution channel, and to customers known to be in the design phase for up to two years before the product discontinuance notification. Final shipments are delivered commensurate with Intel's production capacity.

b) **Product Design (Affects the Fit, Function, or Reliability of the Product)** — This characteristic of change may include but is not limited to board layout, boards and systems BIOS changes, stepping changes, die shrink changes, product packaging changes, or any other change which directly affects the performance of the product.

 The minimum notification window for a product design change is 90 days for components and varies for boards. The notification window commences from the date the PCN is published to the customer until the last ship date as indicated on the PCN milestones.

c) **Manufacturing Site** — This characteristic of change may include but is not limited to proliferation of product to additional FAB and/or Assembly sites, or transfer of product to other FAB and/or Assembly sites.

d) **Product Material** — This characteristic of change may include but is not limited to materials which do not affect the fit, function or reliability of the product sold to customers. Example: molding compounds, lead frame, heat sync, new parts, alternative parts, etc.; any physical portion, entity that goes into a board or system, e.g., brackets, IC's, LED's, assembly material changes, etc. *If the material change affects the fit, function, or reliability of the product, the change should be considered a Product Design change.*

e) **Product Marking** — This characteristic of change describes a change to the marking of the product and not the ingredients or components of that product. Examples may include but are not limited to the methodology used to mark the product (Ink vs. Laser) or a change in content or location of the mark on the product.

f) **Transport Media** — This characteristic of change may include but is not limited to intermediate and shipping boxes, tubes, JEDEC trays, anti-static bags, carrier tape and reels, etc.

g) **Label** — This characteristic of change affects any dimensional or visual change made to any visible labels associated with the product. This includes box labels, transport media labels, etc.

h) **Order Code** — This characteristic of change may include but is not limited to a change in the Intel order code that may be due to a need to segregate pre-conversion to post-conversion material.

i) **Documentation** — This characteristic of change is to be used by Corp. Change Management or their designee to communicate business process changes to methods in how Intel communicates product changes to customers. This will not to be used for communicating spec. updates, changes to data sheets, or any other documentation not related to the PCN communication process.

The minimum notification window for PCNs varies by business group. The corporate guidelines are listed in the tables below.

Key Characteristic of Change	Days of Notification Boards and Systems *	Days of Notification Components*
Product Discontinuance	120	365
Product Design	15	90
Manufacturing Site	15	90
Product Material	15	30
Product Marking	15	30
Transport Media	15	30
Label	15	30
Order Code	15	30
Documentation	15	30

Table 7-1: Minimum Corporate Guidelines for PCN Notification

Key Characteristic of Change	Days of Notification Non-Full Qualification	Days of Notification Full Qualification
Product Discontinuance	N/A	365
Product Design	60	90
Manufacturing Site	N/A	90
Product Material	N/A	30
Product Marking	N/A	30
Transport Media	N/A	30
Label	N/A	30
Order Code	N/A	30
Documentation	N/A	30

Table 7-2: IA CPU Products

Key Characteristic of Change	Days of Notification - Components	
	Embedded	Cellular
Product Discontinuance	546	273
Product Design	90	90
Manufacturing Site	90	90
Product Material	30	30
Product Marking	30	30
Transport Media	30	30
Label	30	30
Order Code	30	30
Documentation	30	30

Table 7-3: Flash Product Group

More PCN information is available through the Intel Product Change Notification System (PCNS) located at http://intel.pcnalert.com.

7.2.4 Order Fulfillment Quality

Order fulfillment quality refers to the quality of ordering and logistics processes from initiation through customer receipt and any issues that involve the order placement and delivery. Order fulfillment quality issues can occur when procedures or processes are incomplete, incorrect, absent, or not followed. The Order Fulfillment Quality (OFQ) program assures the delivery of Intel products and services are complete, on time, and in perfect condition. OFQ issues are assigned to the categories indicated in Table 7-4: Order Fulfillment Quality Definitions.

OFQ Issue Type	Definition
Damage	Shipment received with punctured, crushed, damaged product tubes, trays, reels, bags, and /or boxes.
Electronic Data	Incorrect or missing data transfer from one system to another.
Incomplete Systems/Kits	Shipment received with system parts, kits, or accessories missing.
Labels - Box/Ship	Shipment received with missing, wrong, or damaged labels on packaging or shipping containers. This includes all labels on tubes, reels, trays, bags, boxes, intermediate boxes, and shipping boxes; excludes labels on the actual product.
Miss - Delivery	Entire shipment was not received or a portion of the shipment is missing cartons.
Packing	Tubes, reels, trays, bags, or boxes are not packed per customer's specification.
Paperwork	Packing lists, shipment documentation, Certificate of Compliance and customer specific documentation is illegible, incorrect, or missing.
Wrong Product	The product received was different from what the customer ordered or expected. This includes mixed product, wrong accessories, wrong hardware, and wrong software.
Wrong Quantity	The quantity of units or systems received was more or less than the quantity that the customer ordered or expected.

Table 7-4: Order Fulfillment Quality Issues Definitions

Order Fulfillment Quality Support — Order fulfillment quality is measured Order using a Defects Per Million (DPM) calculation and is monitored through a worldwide database for technical and administrative quality issue management. Performance to goals is monitored and improvements are made through corrective actions and problem solving teams.

Order fulfillment quality issues should be directed to the account Customer Business Analyst or Customer Quality Engineer. The problem resolution process begins when the information is entered into the worldwide database. Then, the organization responsible for the issue resolution will:

- determine the root cause
- implement containment actions
- develop and validate corrective actions
- address systemic corrective actions

The CBA or CQE communicates with the customer regarding the status, root cause and corrective actions.

Customers who buy Intel products from a distributor dealer should contact that distributor for technical support and information services.

7.2.5 Technical Quality

Technical quality refers to the product performance, usability, quality and reliability. Intel product failure during a customers manufacturing or test operation is an example of a technical quality issue. Intel provides customers with problem response and resolution for technical quality issues. Examples of technical quality issues are shown in Table 7-2.

Support and response for technical quality issues are based on customer impact and priority given to a specific issue. One of three priority levels is assigned to Technical Quality issues: High, Medium, and Standard. High priority issues have high impact to the customer. Examples include manufacturing lines down, special rework or product screening, customer not shipping products, serious field failure, or delay of a new product. Medium priority issues are typically routine issues with the possibility of becoming high priority if not responded to in a timely manner. Standard issues are routine issues with no known immediate impact to the customer.

Technical Quality Issue Category	Definition
Miscorrelation	Any unit that passes all tests are defined for that product including the customer reported failure mode.
Test Hole	Any unit that fails a valid test outside of the test program flow.
Customer Induced Damage (CID)	Any failing unit that has been caused by the customer's misuse of the product.
Assumed Reliability Failure	Any unit that fails because of infant mortality or any other reliability determined cause, or any unit that fails Intel's test program, but cannot be assigned to a known category.
Manufacturing Escape	Any defective unit shipped by Intel and detected by the customer, such as bent leads, missed tests, etc.
Fail Analysis Results Indeterminate	Any unit that has an indeterminate root cause and further analysis cannot resolve.

Table 7-5: Technical Quality Categories

Functional Analysis Correlation Request — Intel's engineering support team, together with the customer, determines if physical analysis is needed or if the issue can be resolved in another way. Alternatives could include providing product health data, product support information or returning the failing product for credit without further analysis. Technical Quality issues are handled by Quality Support Centers, which are located in all major geographies to deliver responsive quality support in close proximity to customers. This support model allows customers anywhere in the world to experience service as if they were dealing directly with local factory personnel.

If physical analysis is needed, Intel uses the Functional Analysis Correlation Request (FACR) system to manage the return of the units to Intel and to record the results of the analysis. Customers typically request FACR services to understand failures occurring in their manufacturing process or after shipping to their customers. The FACR process helps determine if failures are due to the Intel product or a problem induced by the customer's use of the product.

The FACR process utilizes product testing, signature analysis, fault isolation and failure analysis techniques. The appropriate level of analysis is determined by Intel and the customer to resolve the issue to the customer's satisfaction. The FACR process:

- Correlates customer perceived failure behavior
- Determines the failure root cause
- Drives appropriate corrective action when Intel caused
- Assists customers to resolve causes of customer-induced failures

For issues requiring the FACR process, the throughput time goals for technical quality issues are as follows:

- Initial response—48 hours for high priority; 5 days for routine quality issues
- Issue closure—24 days for high priority; 30 days for routine quality issues
- Issue to resolution closure—48 days for high priority; 60 days for routine quality issues

Upon closing an FACR, customers are invited to participate in a satisfaction survey to give their feedback on the FACR process. This survey allows Intel to improve effectiveness and customer quality support services.

For more information, customers contact their Intel Field Sales Engineer or Customer Quality Engineer responsible for originating the Functional Analysis Correlation Request (FACR).

7.2.6 Returns Management

The materials return process is different for direct customer and channel customers. For direct customers, we utilize a Return Management Authorization (RMA) process. For Intel's channel customers, we offer a product exchange process.

Direct Customer Return Materials Authorization Policy — The Worldwide Direct Customer RMA Policy identifies three categories of returns:

Administrative — Non-technical returns authorized by Intel caused by an administrative error made by Intel, such as, but not limited to, wrong product shipments, order entry errors, duplicate orders, over-shipments, wrong destinations, and wrong shipping dates.

Technical in-warranty — Returns of defective product made within the product's warranty terms and conditions.

Technical out-of-warranty — Returns of defective product or product to which the customer desires to have work done (e.g., upgrade to latest revision), but not covered within the product warranty terms and conditions.

Channel Warranty — The worldwide Channel Warranty Program policy offers two levels of programs:

Standard warranty program — Customer contacts Intel for authorization. Upon Intel receipt of the defective product, Intel dispatches replacement product.

Advanced warranty program — Customer contacts Intel for authorization. Intel dispatches a replacement part to the customer, and the customer returns the defective part to Intel.

Business rules defined by Intel Channel Management determine access to the standard warranty and advanced warranty program, including quantity limits. All product warranty returns are subject to Intel's business terms and conditions.

Warranty Returns Process — Customers may request support on warranty returns for defective product. Warranty periods may vary by product. Intel's Returns Management Center maintains records characterizing warranty period and terms by product.

For **direct customers**, requests for warranty returns should be directed to the regional returns management offices or using Intel Business Link (IBL) web-based tool. Support on returns can also be provided via the account team and the Customer Quality Engineer (CQE).

For **channel customers**, returns are coordinated through the Channel Warranty Program. For specific details visit www.intel.com/reseller and select technical support. Warranty requests can be submitted by email, web tools, or telephone. For a listing of telephone numbers, visit www.intel.com/reseller and select contact support.

Technical In-Warranty Returns are approved at Intel's discretion. Intel offers the repair, replacement, or credit services that are subject to eligibility criteria and vary by geographic region.

To validate eligibility, customers must provide proof of purchase information (such as the invoice) or serial number information for products being returned. Customers must also identify the technical reasons for the product return. Returned products may be screened and tested by Intel.

If the product is determined by Intel to be Customer Induced Damage, No Defect Found, or Out-of-Warranty, Intel reserves the right to take one or more of the following actions:

- Deny request for credit or replacement
- Reverse any credits which might have been issued already for the product
- Return the material at the customer's expense

7.2.7 Measuring Customer Satisfaction

Intel's 'Customer Excellence Program' (CEP) measures overall customer satisfaction and drives corporate or business unit improvement actions. This program uses a third-party market research firm to obtain statistically relevant feedback on Intel's products, processes, and programs through a web-based survey. The survey covers a range of customer job functions and supports multiple languages, asking questions that are most relevant to the job role of each participant.

Through the Intel CEP, we elicit and listen to our customer's feedback to:

- Take a holistic approach to understanding and improving customer satisfaction
- Obtain statistically relevant and actionable data from a variety of business touch-points within customer accounts world-wide
- Prioritize and drive identified high-impact issues to resolution while ensuring communication of our actions and results back to our valued customers

- Continuously measure and improve Intel customer satisfaction and preference across every geography and channel
- Reinforce a company-wide customer orientation focus

Survey Analysis — Once customer feedback has been collected, in-depth data reviews and regression analyses are performed. This provides multiple views across customer accounts:

- A broad level view indicates overall customer satisfaction and future commitment
- A business level view measures satisfaction in areas such Intel's technological innovation, value-add services, and attributes such as responsiveness and product features and performance.
- A detailed view to help identify specific customer concerns or issues.

Responding to Issues — Intel Executive Management reviews survey analysis findings and sets the corporate focus for company-wide action and resolution of high-impact customer issues. A well-established issue management and response processes is used to drive resolution to CEP issues and the owning organizations make certain that priority is given to high-impact issues. Existing efforts may be reinforced or redirected based on the survey results. The results of these actions are then communicated back to customers through sales, marketing, quality or other communication channels.

8. Synopsis

Intel implemented a flexible Quality Management System architecture based on Intel's Mission, Corporate Values, and Quality Policy. The QMS utilizes four key elements: 1) Plan, 2) Organize, 3) Execute, and 4) Monitor. These elements adapt quickly and effectively to new business trends in order to satisfy customers' changing needs for quality and reliability in products and services. This architecture encompasses a wide range of mature and robust systems and processes, and enables Intel to provide responsive support to customers and optimize the customer usage of Intel products.

Intel's quality documentation system consists of corporate business principles, group guidelines, governing specifications, and operational policies, guidelines, and procedures. These provide output that creates value for customers and stakeholders, and enables profitability and growth for Intel.

Intel manages quality throughout Technology Development, Product Development, Materials Quality, Manufacturing, and Customer Support. Each of these operations depends on the quality management and quality delivery of the other.

Technology Development enables Intel products to provide better value, through improved performance, increased functionality, or smaller size. Product Development uses processes to take a product from market research through production, and eventually to product discontinuance. Materials Quality provides materials and services for production to meet agreed-upon requirements, lead times, and pricing. Manufacturing enables quality production by understanding customer quality requirements and implementing processes that help ensure operations meet these requirements. Customer Support provides customer assistance by understanding, documenting, analyzing, and resolving customer issues.

Intel uses each generation of technology to manufacture a large number of products. Therefore, it is crucial to ensure that each core technology exhibits high quality and reliability. At Intel, the term 'qualification' refers to the quality and reliability assessment of a particular product, and the term 'technology certification' refers to the quality and reliability assessment of a core technology.

From Pathfinding through Deployment, Intel uses standard and custom tests to address the challenges inherent in the rapid advancement of electronics core technologies. This systematic approach enables Intel to ensure that high quality technologies are developed along the path to production. Intel bases the development of technology on planning and certification for silicon, package, sort/test, and boards.

Silicon Technology is the fabrication process used to create the IC on silicon wafers by adding and patterning the layers that form transistors and interconnects. Intel certifies a process technology when it meets quality and reliability goals, and a lead product has been manufactured on the technology and shown to meet requirements.

Package Technology is the assembly process used to enclose the silicon IC in an electronic package with connections accessible to the user. Increasing product and market performance needs drive process and design development for package, assembly, and enabling processes. New products typically require feature size reduction and added design complexity to accommodate improved functionality and increased electrical requirements.

Sort/Test Technology is the test process, from wafer sort through package-level test and burn-in, designed to ensure that shipped devices meet datasheet requirements. The primary reasons Intel performs tests are to ensure proper functionality of the product at the required speed and to assure the products customers receive meet Intel's quality goals. Test processes also provide valuable feedback to the upstream silicon and assembly processes, often detecting subtle variations that change product performance parameters such as, defect density, frequency, power, etc.

Board Technology consists of the design and fabrication of printed circuit boards or motherboards that enable integration of individual components. Ever increasing demands for higher product performance drive Board technology development and certification. Certification activities include the validation of new enabling components and thermal solutions, as well as board reference designs. Advancements in silicon technology act as the primary driver of board technology developments.

Once a technology has been developed, the next step is to create a product based on that technology. The Product Development organization utilizes the Intel Product Qualification System and Product Life Cycle to take a product from market research through production and eventually to product discontinuance. The Product Qualification System provides the framework to apply the product quality and reliability requirements, develop and apply engineering solutions, validate product performance, deliver meaningful collateral to our customers, and release healthy products. The Intel Product Life is an integrated approach to product planning, development, manufacturing, support, and discontinuance, involving all operations and levels of the organization. It has four phases major phase, Exploration, Planning, Development, and Production, with management approvals required to move from one phase to the next.

Intel tracks the advancement of qualification activities through the PLC phases and associated milestones. Nine qualification milestones shape requirements, establish development expectations, and drive conformance to those requirements, resulting in qualified products. The inherent quality, compatibility, and robustness of our product and platform designs are major aspects of delivering to the Intel brand promise.

At Intel, Validation refers to the process devoted to proving out our product and platform designs. It is important to ensure that the product successfully transfers and ramps into manufacturing. Intel's qualification methodology relies on assessments using process and product matching, and product-specific process control systems.

By integrating the Product Life Cycle and the Product Qualification System, Product Development quality and reliability personnel meet customer needs through early customer and market engagement, innovative engineering, thorough validation, and world-class manufacturing.

Materials quality is a key consideration in all stages of the product life cycle starting with new material discovery, characterization and eventually, certified material that is used in the manufacturing sites. Stable and predictable quality, availability, and cost effectiveness of incoming material are critical and necessary conditions for Intel factories to run smoothly and deliver products that meet customer satisfaction. The Materials Group works closely with the supplier and collaborates in Intel's Supply Chain to accomplish this mission. The Materials Quality Operating System (QOS) is the approach employed to achieve the quality objectives in each of the four QOS platforms.

The Supplier Selection platform defines the needs and assessment criteria for selecting and developing the best supplier. Next, the Supplier and Materials Qualification Platform certifies the supplier and qualifies the materials. This platform provides the necessary supporting data and validation to show that Intel system requirements and product specifications are met and determined risks are understood and reduced. The Process Control System and Excursion Management Platform allows the supplier to prove its ability to prevent, detect, and respond to issues, such that Intel and Intel's customers are minimally impacted by discrepant material found by the supplier. In the Supplier Continuous Quality Improvement Platform, Intel works closely with supplier to track and communicate supplier performance, address current and potential issues, and identify opportunities for further improvement. This platform enables the supplier to consistently meet Intel expectations and have a competitive advantage in the industry.

Intel uses the same Materials QOS approach with subcontractors, such that their products meet Intel form, fit and function specifications and are equivalent to those from Intel factories. Essentially, suppliers and subcontractors managed by proven Materials QOS methods and tools deliver products and services that meet, and sometimes exceed, the expectations of Intel and Intel's customer.

Manufacturing uses issue prevention as its main approach in providing quality products. This is evident in the use of the Intel Copy Exactly! Methodology and manufacturing systems. Intel's Copy Exactly!, a methodology followed by Fab, Sort and Assembly Test Manufacturing, focuses on matching the manufacturing site to the development site. Copy Exactly! benefits include faster production ramps for enhanced product availability and improved consistency to quality performance. Manufacturing systems such as environmental citizenship, process transfer, the use of statistical techniques, the manner of new equipment qualifications, manufacturing monitors, and control systems, and the control of inspection, measurement, and test equipment also aid in issue prevention. If issues are unpreventable, Manufacturing focuses on detection and containment of these issues. The systems in place to enable detection and containment of issues include traceability, manufacturing equipment matching and qualification, process control systems, and best-known methods. Traceability is an identification method that includes lot-tracking numbers that allow forward and reverse traceability of products. Record retention guidelines ensure lot history maintenance. Intel's traceability system enables product identification and tracking through all stages of manufacturing, storage, and shipment to the first point of sale. Manufacturing equipment matching and qualification consists of matching the new tool to a reference tool using sequential statistical methods that allow the equipment to be qualified as soon as matching is demonstrated. Manufacturing rarely encounters any equipment issues because of the meticulous matching process. Reduction of variation and various process control systems and best-known practice sharing across factories also enable the detection and containment of unpreventable issues.

Manufacturing also validates through various forms of audits and assessments focusing on quality culture and business processes. Internal quality system audits provide an evaluation of whether or not the existing requirements are met. Internal auditing evaluates processes and systems for effectiveness and efficiency and identifies opportunities for continual improvement. Sites and operations perform annual self-audits of their quality system and processes. Self-audit teams, comprising functional content experts, train on basic auditing methods and techniques as well as ISO 9001.

Primarily, Intel's Customer Quality Support Network provides post launch support. The Intel Customer Quality Support Network's portfolio of value-add service and support ensures ongoing support to our customers. These services include Materials Declaration, Manufacturing Enabling, Product Change Management, Order Fulfillment Quality, Technical Quality, and Returns Management.

Materials Declaration data sheets provide the necessary material composition information on restricted and banned substances. Intel's Manufacturing Enabling program results in the successful product launch of new technologies at customer sites. The outcome of successful launches is higher yields and improved quality and reliability.

Communicating changes to customers and ensuring their readiness to receive enhanced product are key elements of Intel's Product Change Management system. Intel's change notification objectives are to ensure that critical information is communicated, including expected customer impact, provide sufficient evaluation time, enable fast and controlled factory launches, product enhancements, and process improvements for customers.

Order Fulfillment Quality refers to the logistics management of customer orders from initiation through customer receipt, including issues that involve the order placement and delivery. The objective of the OFQ program is to ensure world-class order fulfillment quality that results in Intel products and services delivered complete, on time, and in perfect condition.

Intel's Technical Quality objective is to assure world-class product quality that meets the committed market warranty and lifetimes. Intel provides customers with rapid problem response and resolution. Intel manages two fundamental Returns Management processes for its customer base. For direct customers, Intel offers a Return Management Authorization (RMA) program, and for channel customers Intel offers a product exchange program.

Additionally, Intel listens to customers through daily interactions and through the Customer Excellence Program (CEP). Intel internalizes customer feedback and uses it for continuous improvement of services and customer satisfaction. Intel strengthens customer devotion by using customer feedback to enable strategic investments in our products, brand, and services.

Intel's Quality Policy is that business results are the ultimate measure of success, and the results prove that Intel's Quality Management System works. Intel's Quality Management System provides the architecture through which Technology Development, Product Development, Materials Quality, Manufacturing, and Customer Support fulfill the commitment to providing customers with quality products and services alluded to in Intel's Mission, Corporate Values, and Quality Policy.

Our ability to maintain world-class leadership in technology and performance depends on our commitment to our corporate values of Operational Excellence, Continuous Improvement, and Customer Satisfaction. These values mesh with Intel's policy of striving to maintain the highest standards, ship products that meet our stated goals, quickly communicate with customers, and act to resolve problems. Intel places achieving and maintaining world-class quality leadership as top priorities, creating systems and architectures to achieve this goal, resulting in a quality culture that keeps us at the forefront of semiconductor technology today and tomorrow.

9. References

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